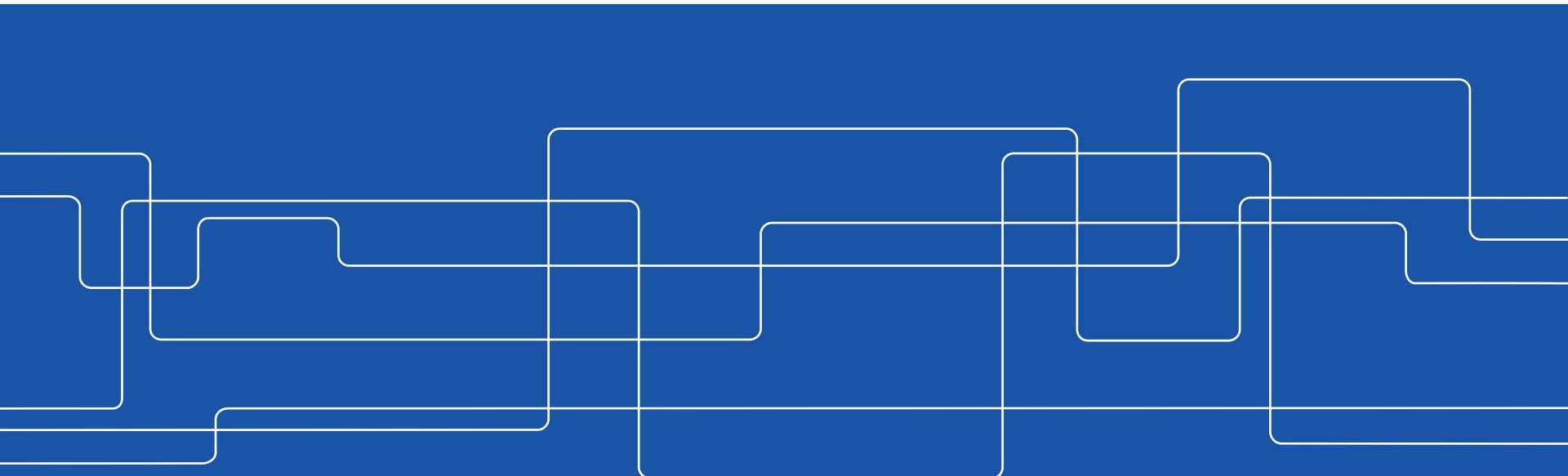




Unconventional Micro-Manufacturing and Integration Technologies

Frank Niklaus





Outline

- Background
- Micro-Manufacturing and Integration Research
 - Heterogeneous 3D Integration for MEMS & NEMS
 - Integration and Packaging for MEMS
 - Nanofabrication Technologies and Graphene NEMS
- Summary



KTH Royal Institute of Technology

Sweden's largest technical university:

- More than 13,000 full-time students.
- Close to 1,800 research students.
- Around 3,500 full-time positions.





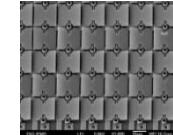
Department of Micro- and Nanosystems

Head: Prof. Göran Stemme



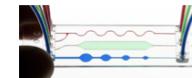
- Micro and Nanosystem Integration

Prof. Frank Niklaus



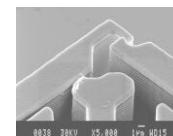
- Lab-on-a-Chip and Polymer Devices

Prof. Wouter van der Wijngaart



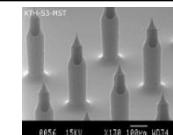
- Microwave and THz MEMS

Prof. Joachim Oberhammer



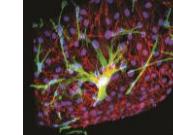
- Biomedical Devices

Assoc. Prof. Niclas Roxhed



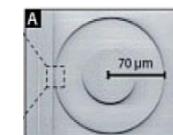
- Bioelectric Hybrid Systems

Ass. Prof. Anna Herland



- Photonic MEMS

Ass. Prof. Kristinn Gylfason





Thanks to all Colleagues at KTH !

Support

- Erika Appel Admin. Ass.
- Ulrika Pettersson Admin. Ass.
- Mikael Bergqvist Technician
- Cecilia Aronsson Technician

Researchers

- Göran Stemme Prof.
- Wouter van der Wijngaart Prof.
- Joachim Oberhammer Prof.
- Niclas Roxhed Assoc. Prof.
- Kristinn B. Gylfason Assis. Prof.
- Anna Herland Assis. Prof.
- Hans Sohlström Assoc. Prof.
- Tommy Haraldsson Researcher
- Ilya Anoshkin Researcher
- Oleksandr Glubokov Researcher
- Jonas Hansson Researcher
- Petr Makhlov Researcher
- Umer Shah Researcher
- Simon Bleiker Researcher



PhD Students

- Stephan Schröder
 - Serguei Smirnov
 - Fritzi Töpfer
 - Alexander Vastesson
 - Xuge Fan
 - James Campion
 - Valentin Dubois
 - Alessandro Enrico
 - Jessica Liljeholm
 - Linnea Gustafsson
 - Miku Laakso
 - Carlos Errando Herranz
 - Emre Iseri
 - Staffan Johansson
 - Aleksandr Krivovitca
 - Laila Ladhani
 - Maoxiang Guo
 - Weijin Guo
- Gabriel Lenk
 - Floria Ottonello Briano
 - Simone Pagliano
 - Arne Quellmalz
 - Mina Rajabi
 - Federico Ribet
 - Xiaojing Wang
 - Reza Zandi Shafagh
 - Zhou Xiamo
 - Zhao Xinghai



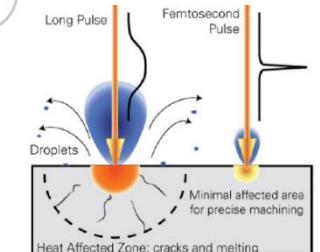
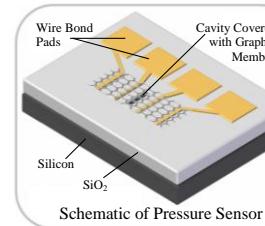
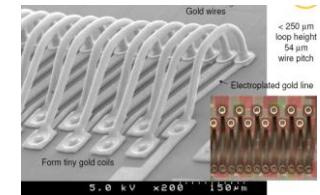
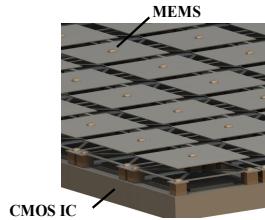
Micro and Nanosystem Integration Group

- 8 Ph.D. students at MST
- 2 industrial Ph.D. students at SenseAir and Silex Microsystems
- 1 postdoc and 3 contributing senior researchers



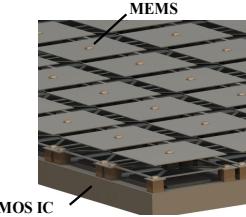
Four Research Topics

- **Heterogeneous 3D Integration Technologies for MEMS and NEMS**
- **Integration and Packaging for MEMS**
- **Nanofabrication Technologies and Graphene-Based NEMS**
- **Femtosecond Laser-Based Micromachining for MEMS & NEMS**



Research Topics in Group

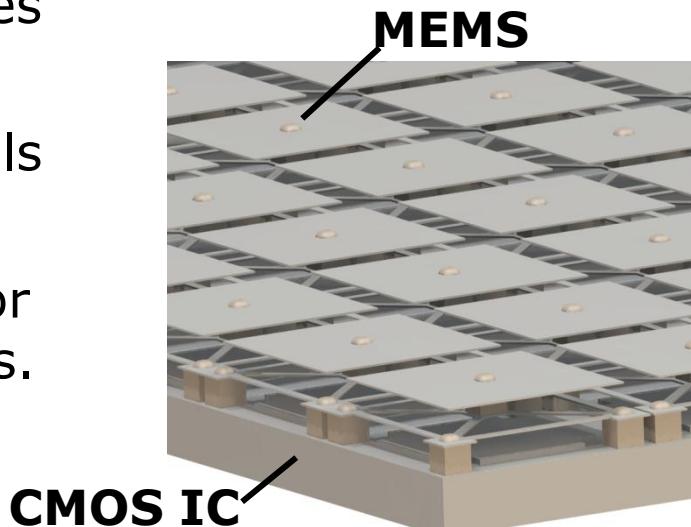
- Heterogeneous 3D Integration for MEMS & NEMS
- Integration and Packaging for MEMS
- Nanomanufacturing Technologies and Graphene NEMS



Heterogeneous 3D Integration for MEMS & NEMS

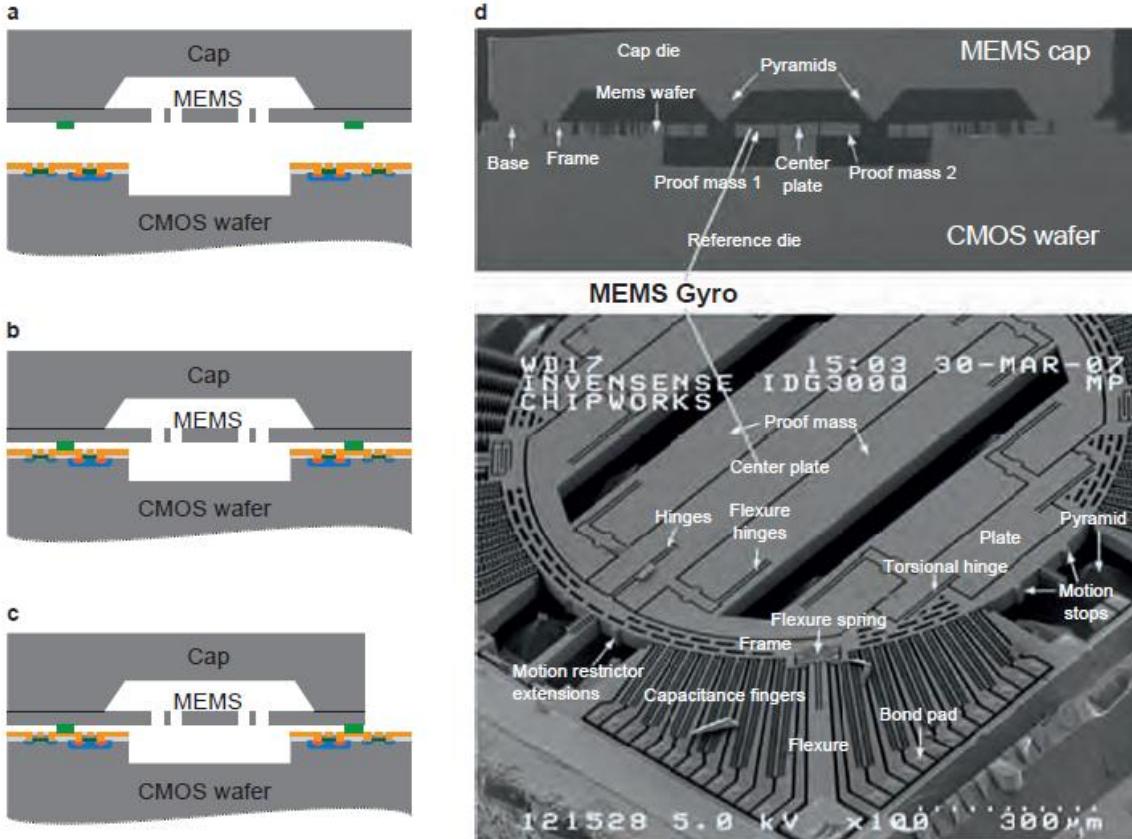
Motivation

- New MEMS designs, functionalities and material combinations.
- High performance MEMS materials on standard foundry ICs.
- Very high integration densities for smaller and cheaper components.

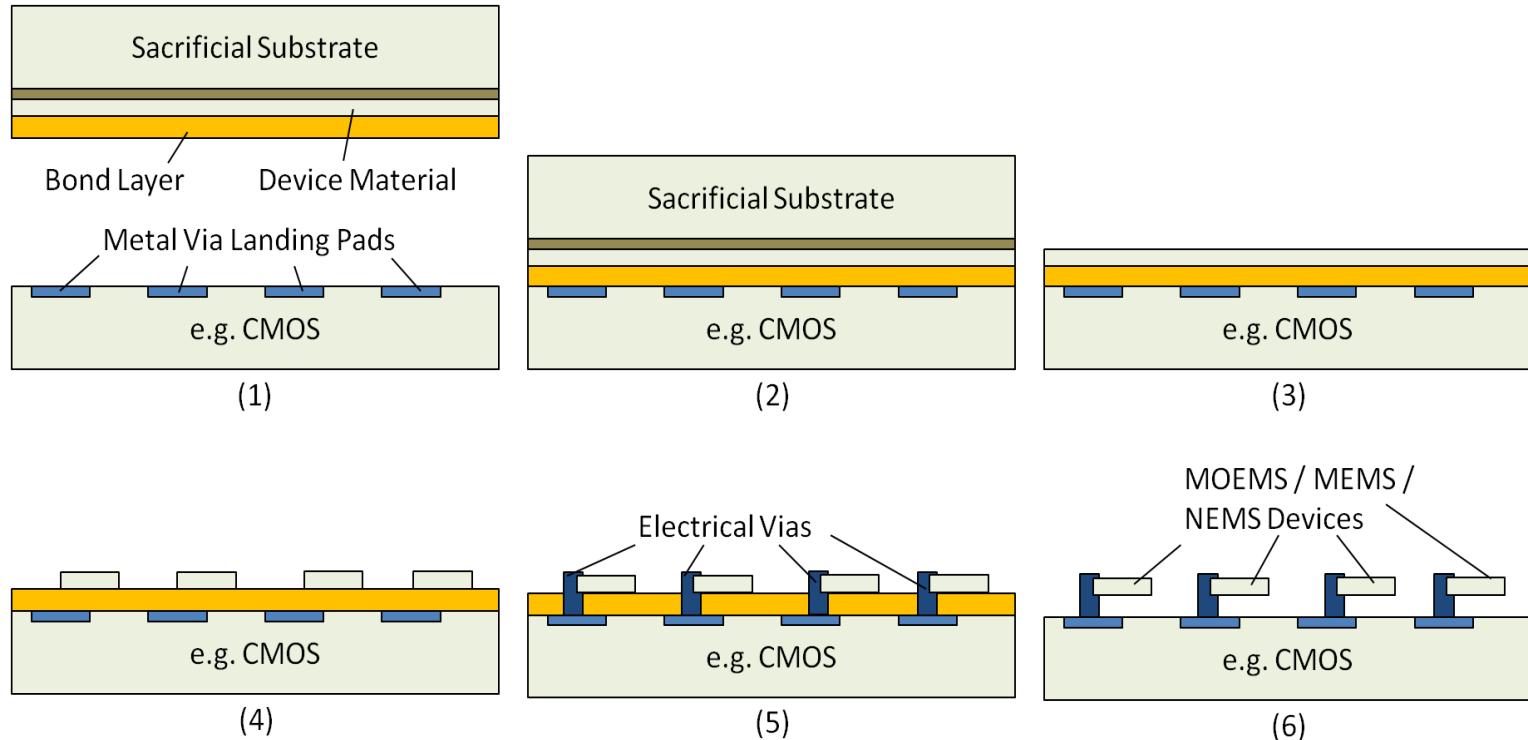


3D Integrated MEMS on ICs

Commercial Examples: Invensense (gyro), mCube (accel.)



Via-Last Heterogeneous 3D Integration Platform

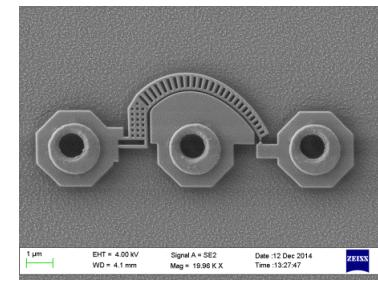
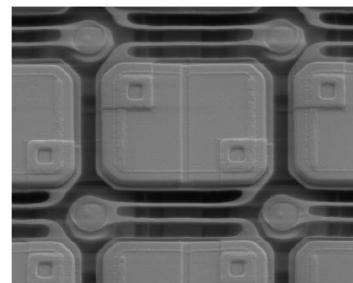
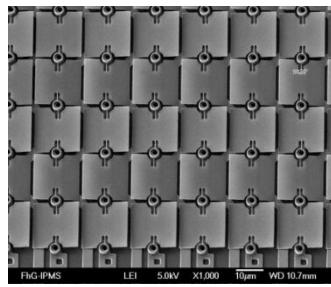


Advantages

- No wafer-to-wafer alignment.
- Extreme reduction of via and dimensions (sub μm) possible.

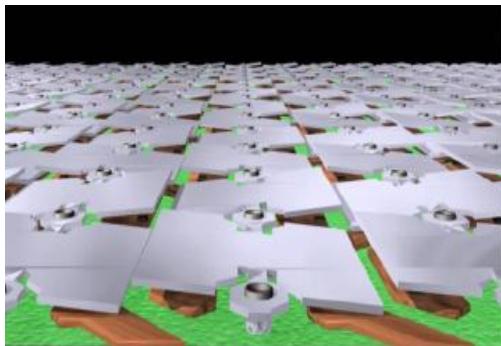
Implemented Applications

- Si Micromirror Arrays
- IR Bolometer Arrays
- NEM Relays

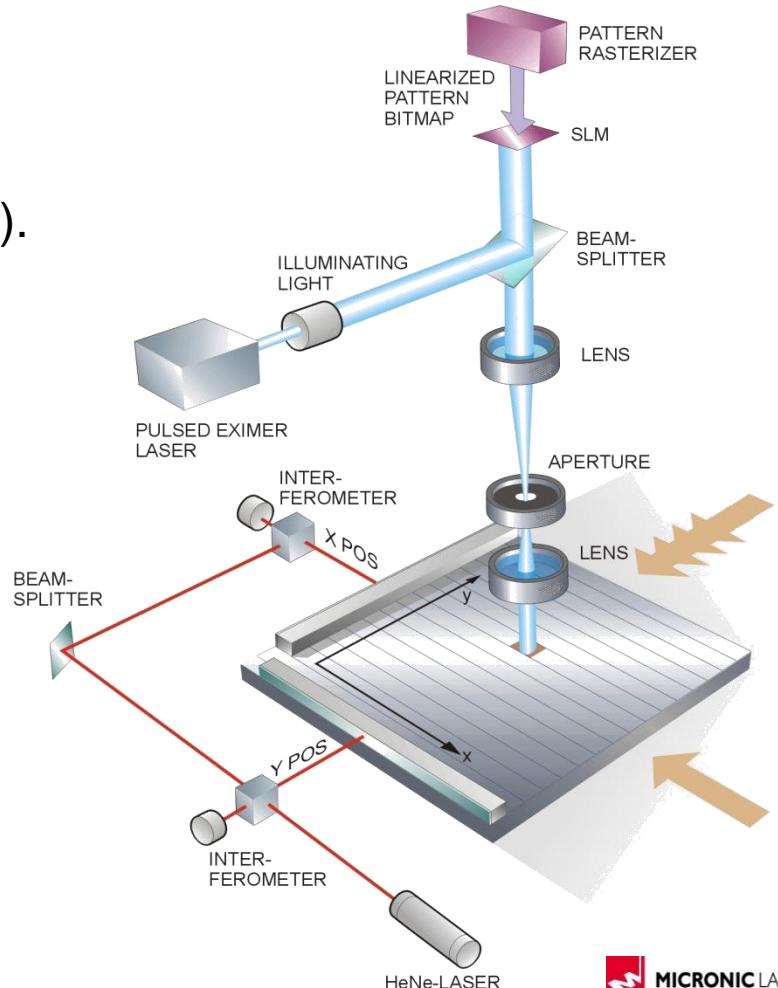


Tilting Micro-Mirror Arrays (SLMs) for Maskless DUV Lithography Systems

- Step and repeat maskless lithography.
- 1 million mirrors (mirror size $16 \times 16 \mu\text{m}^2$).
- Single mirror actuation with underlying CMOS.
- Analogue tilt actuation in 16 steps (gray-tones) possible.

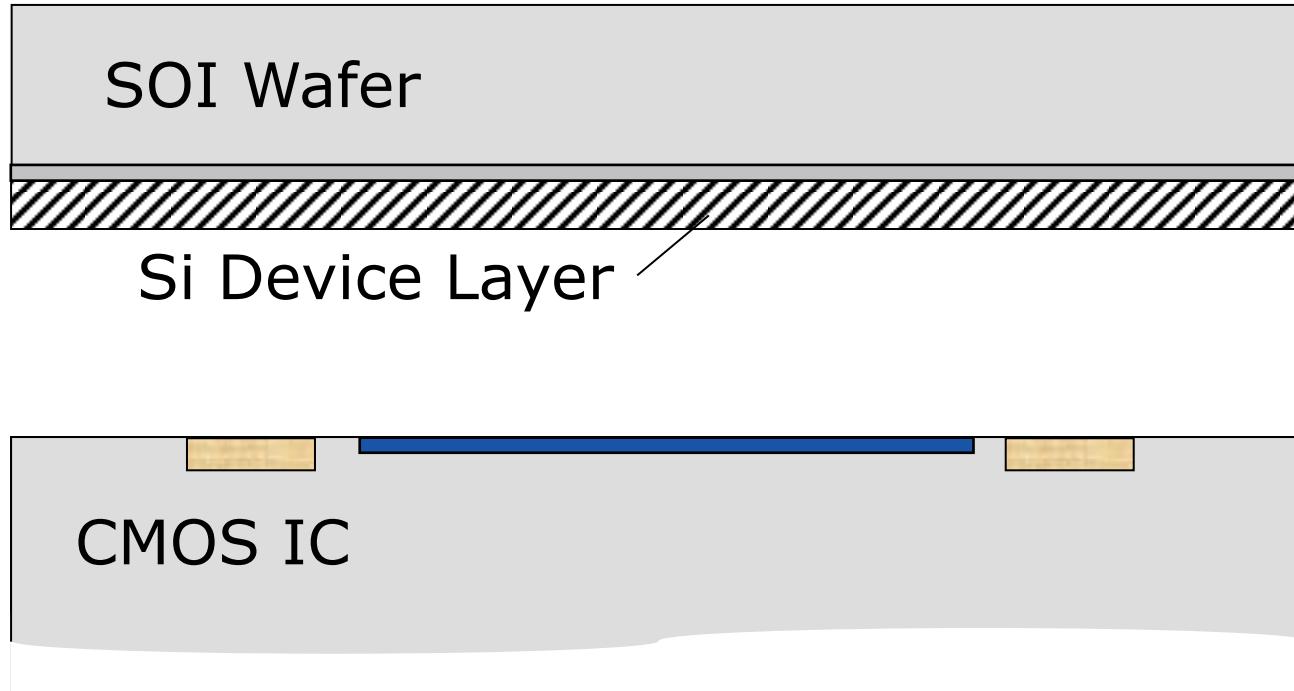


Source: Zimmer, Fraunhofer IPMS



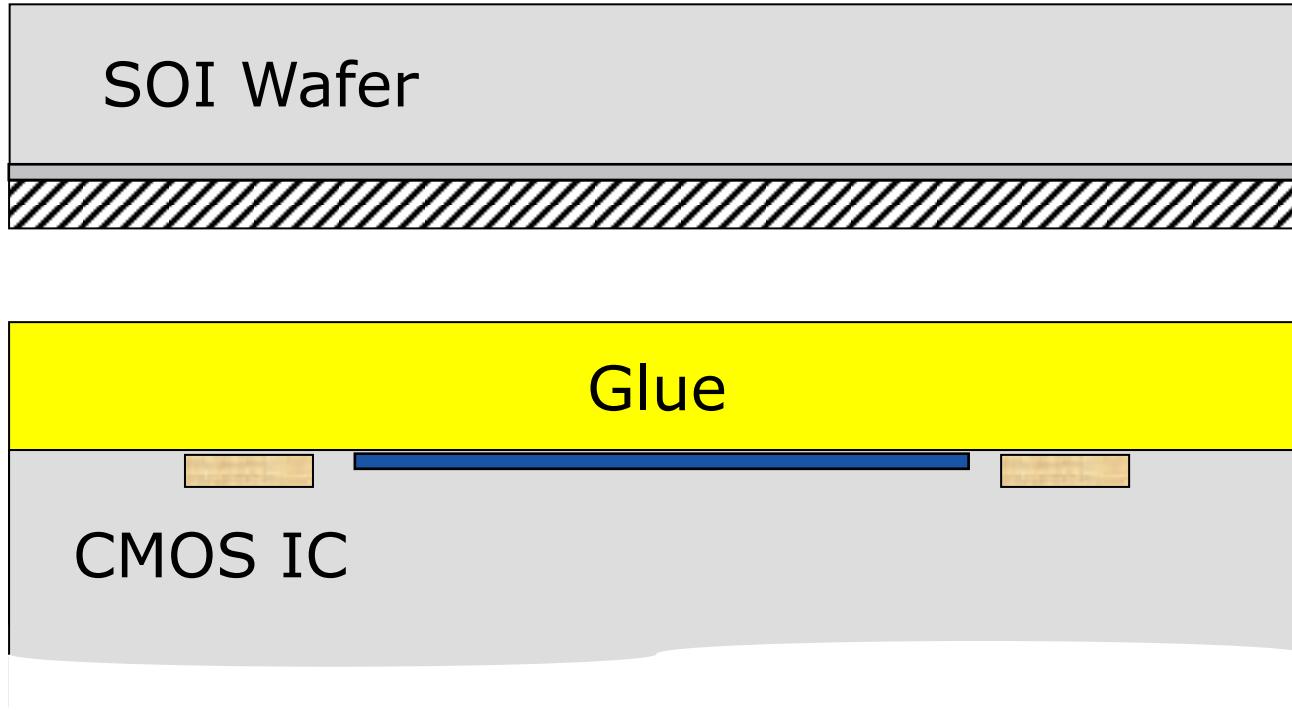


Via-Last Heterogeneous Integration for Mono-Crystalline Si Mirrors on CMOS



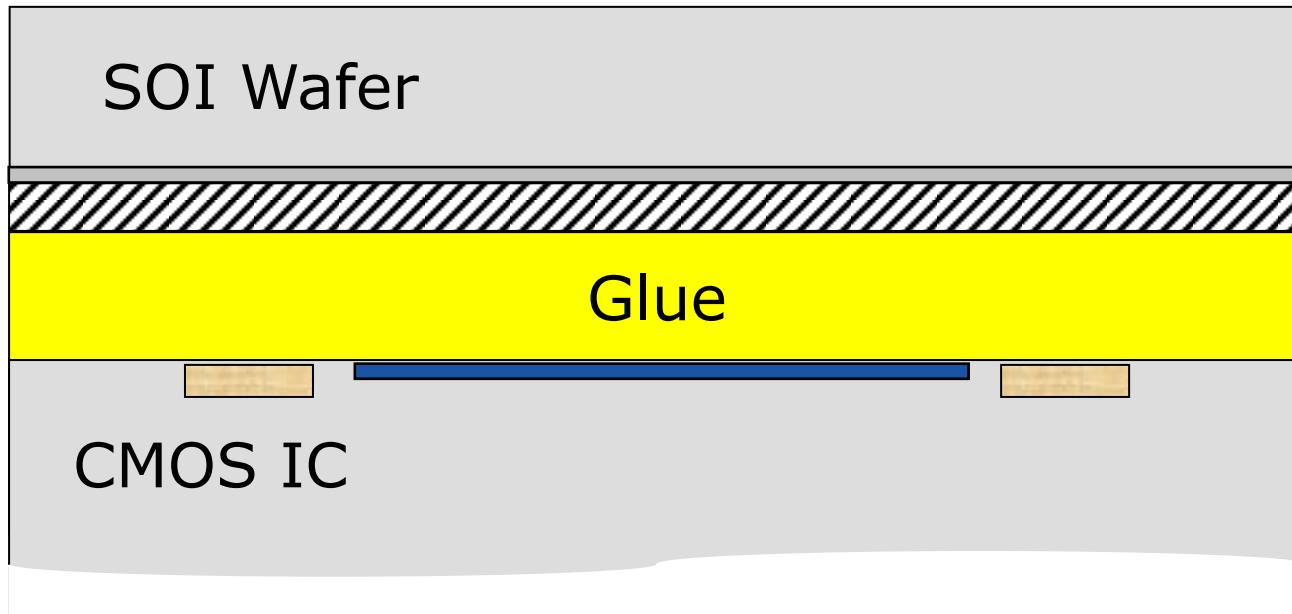


Si Mirror Integration: Dispense Glue



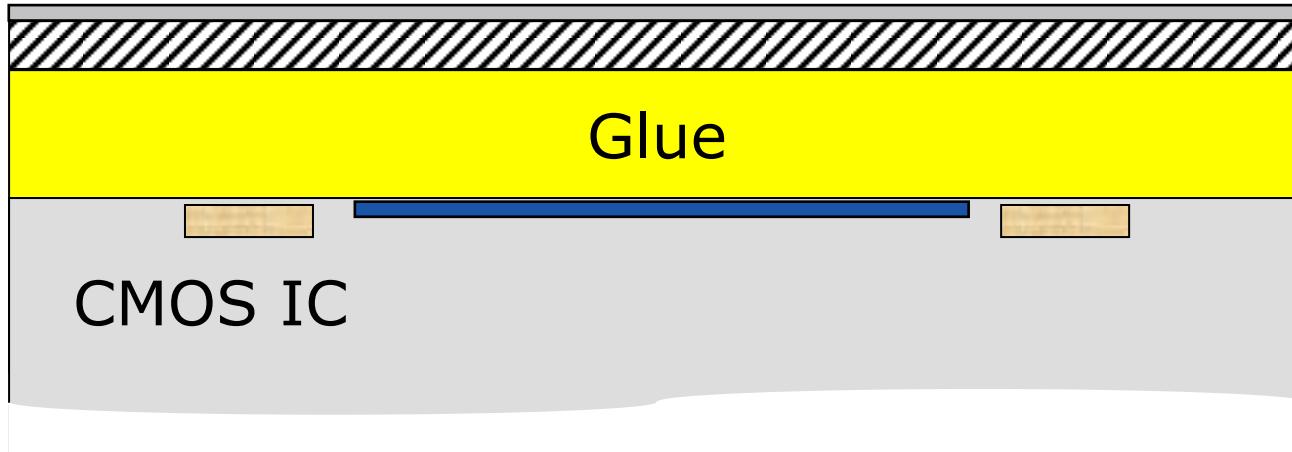


Si Mirror Integration: Adhesive Wafer Bonding

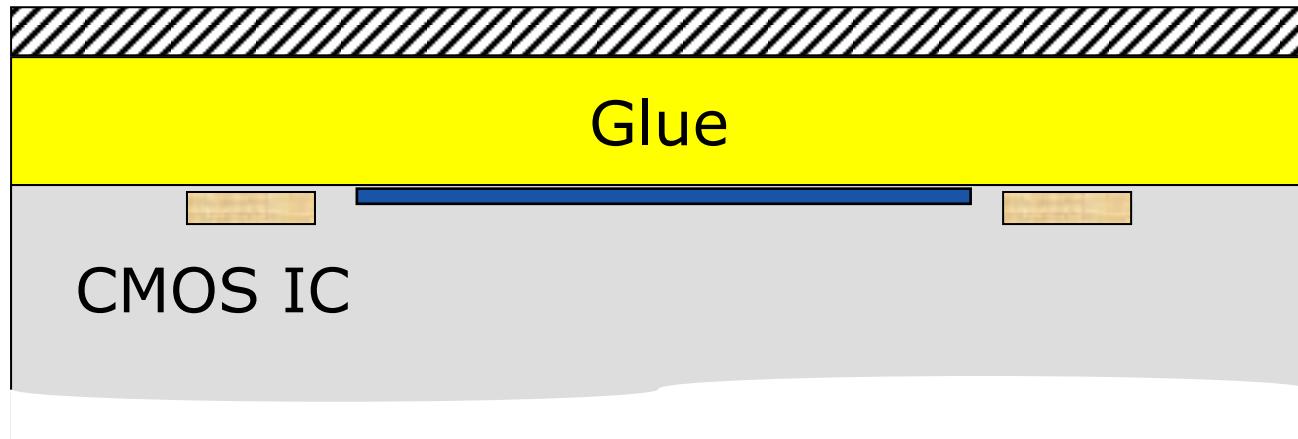




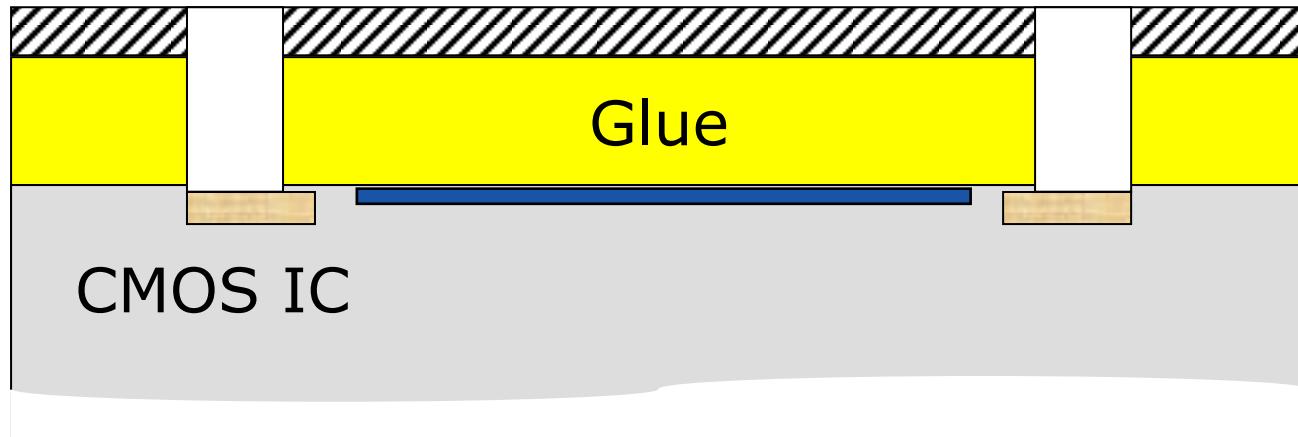
Si Mirror Integration: Sacrificial Wafer Thinning



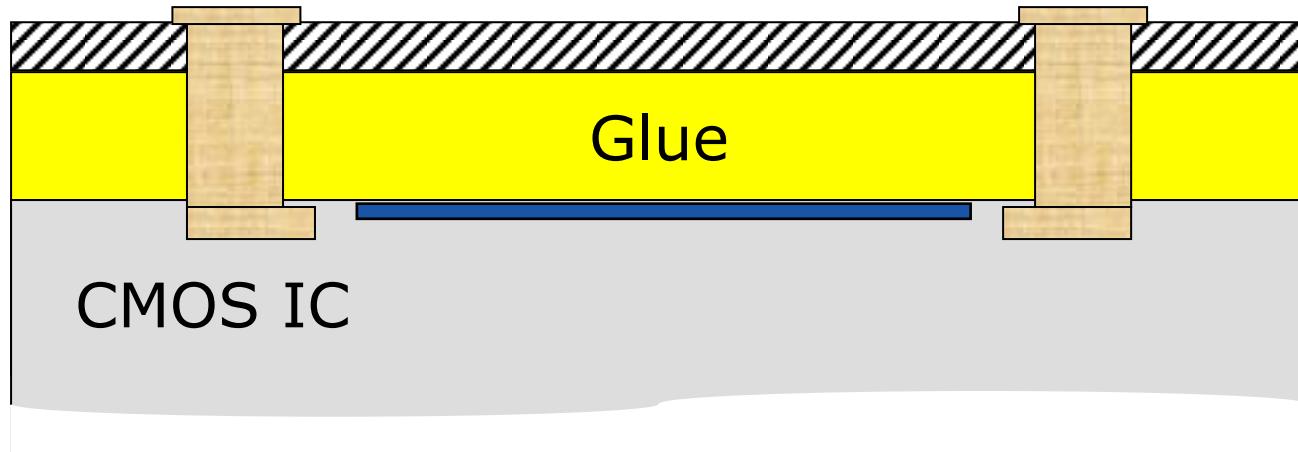
Si Mirror Integration: Removal of SiO₂ Etch-Stop



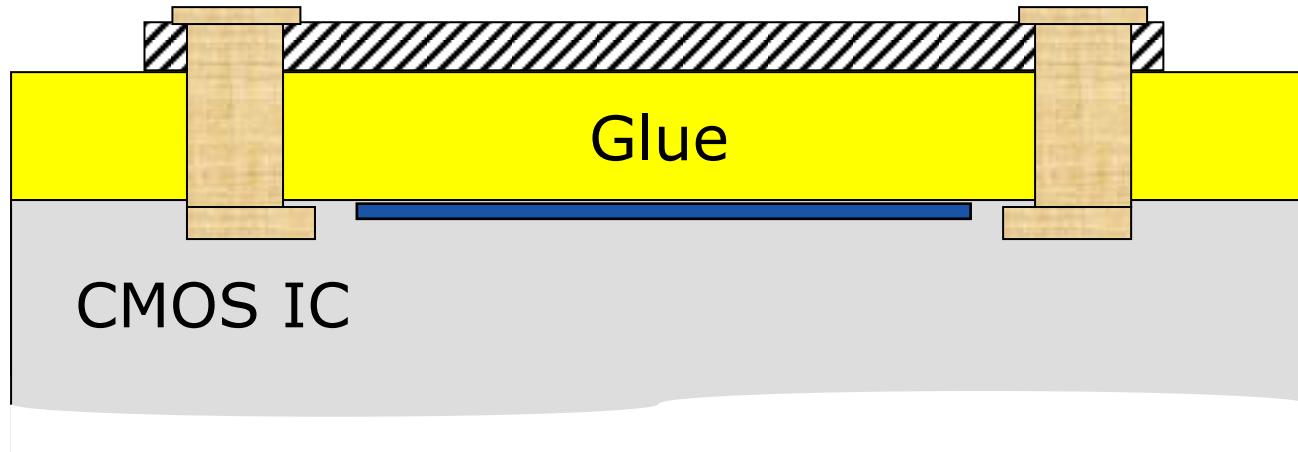
Si Mirror Integration: Via Etch



Si Mirror Integration: Via Formation

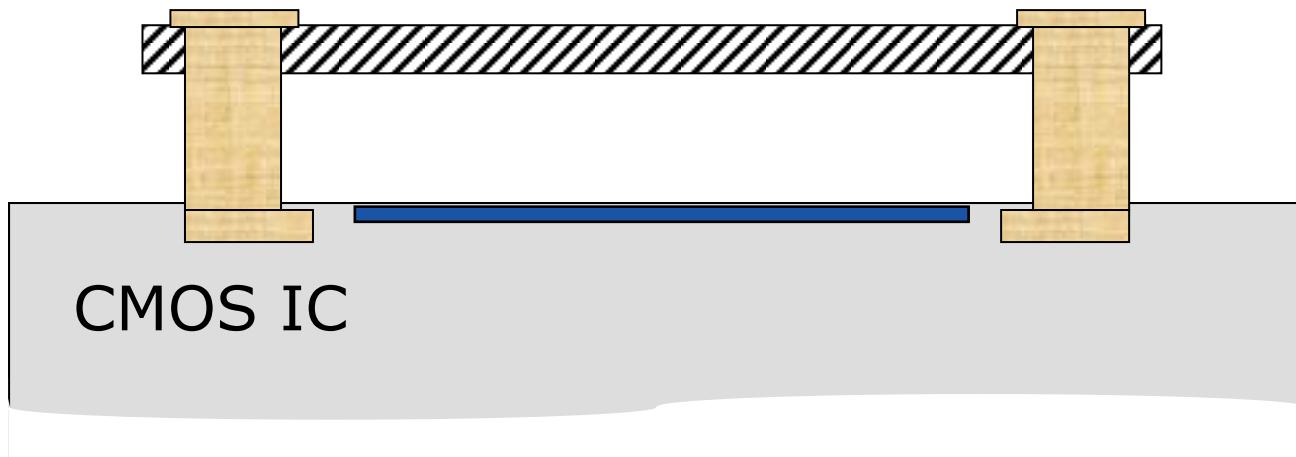


Si Mirror Integration: Mirror Formation



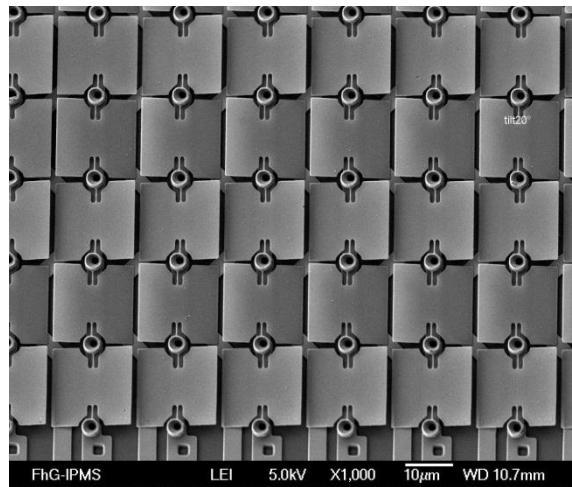
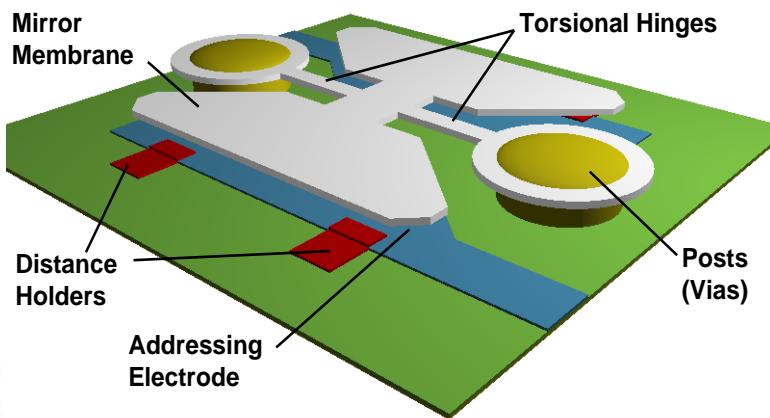
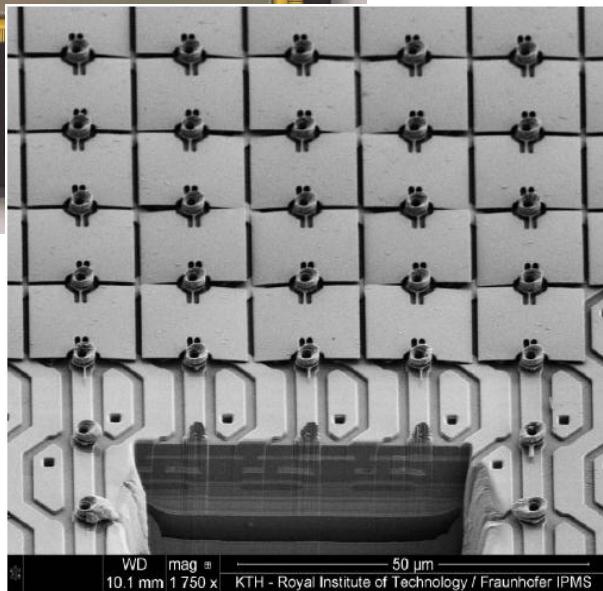
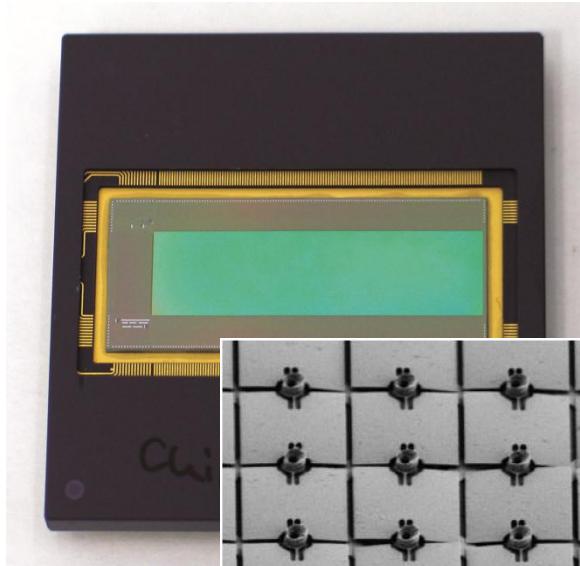


Si Mirror Integration: Mirror Release



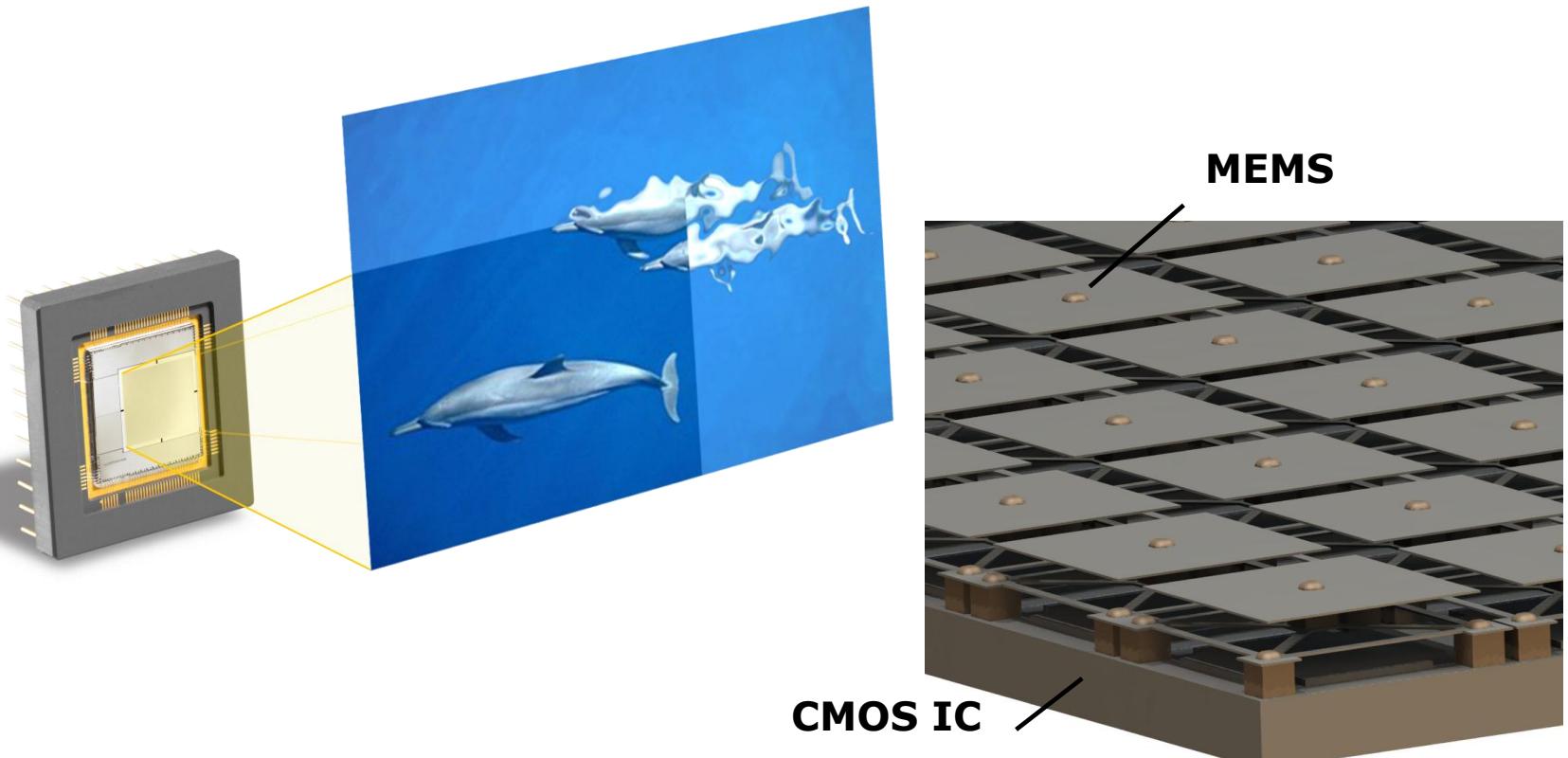


1 M-pixel Mono-Si Mirror Array on CMOS



SLMs for Adaptive Optics in Astronomy and Microscopy

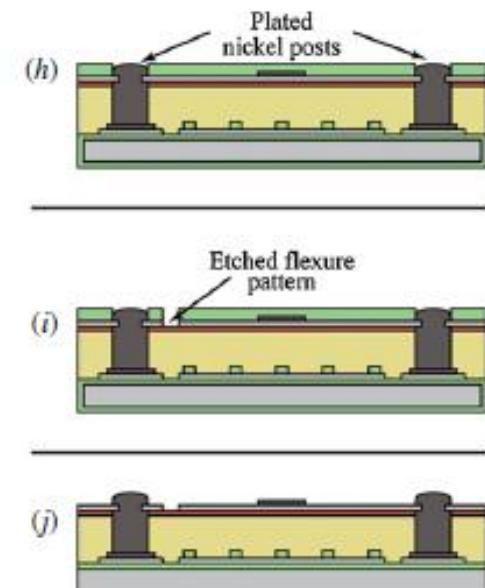
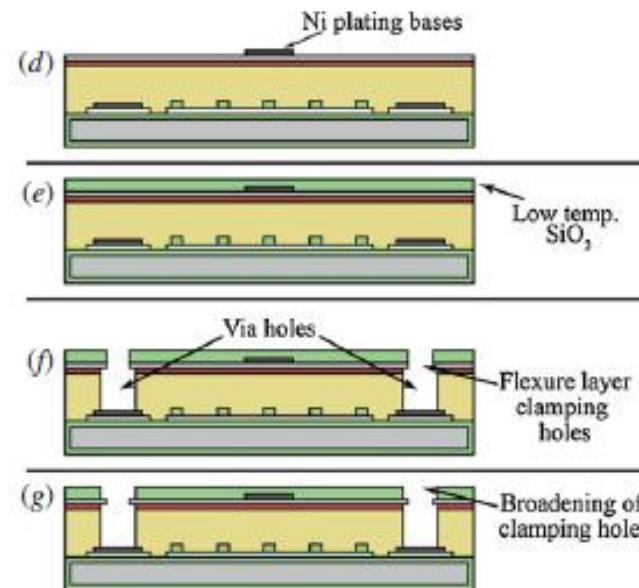
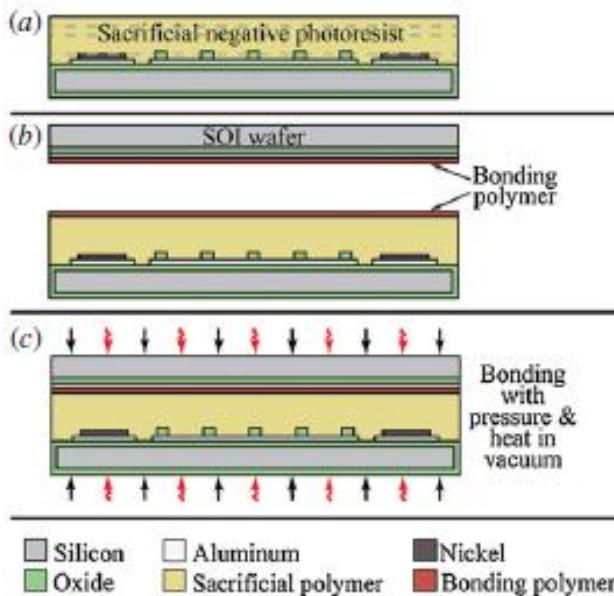
Wave-front correction using piston-type mirror arrays



Source: Lapisa, KTH and Zimmer, Fraunhofer IPMS

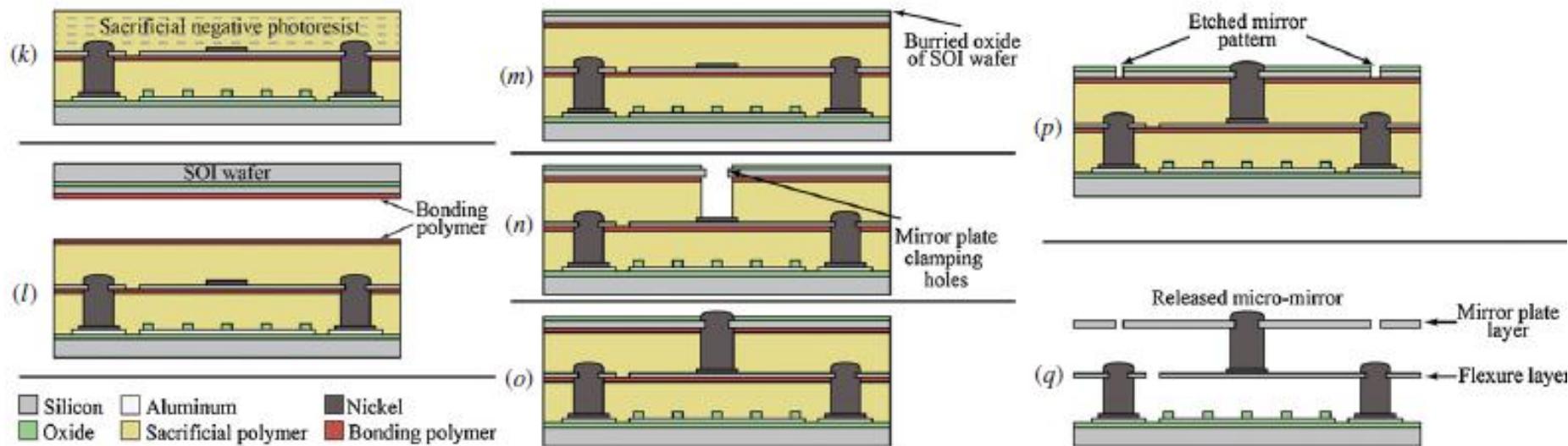
2-Layer SLMs Fabrication Process

1st heterogenous 3D integration sequence

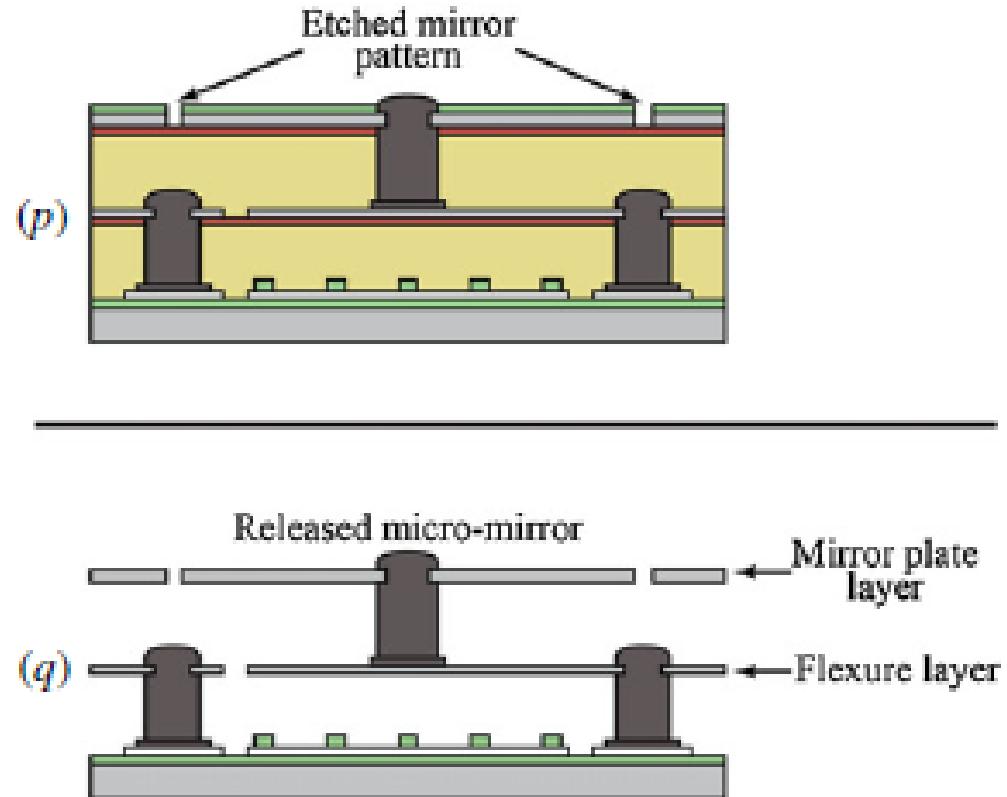
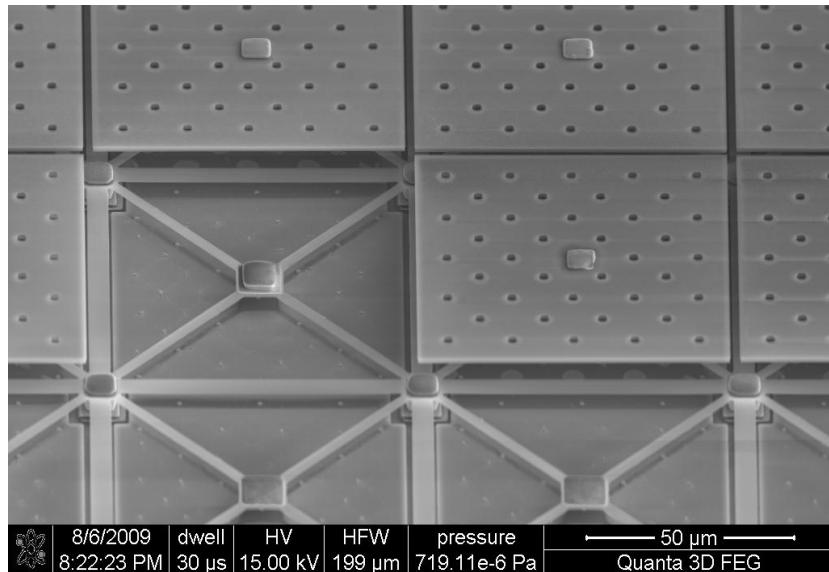


2-Layer SLMs Fabrication Process

2nd heterogenous 3D integration sequence



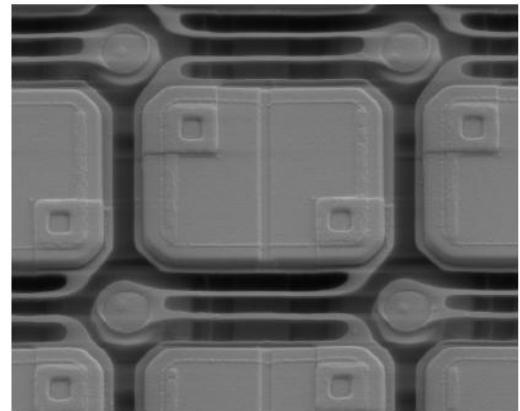
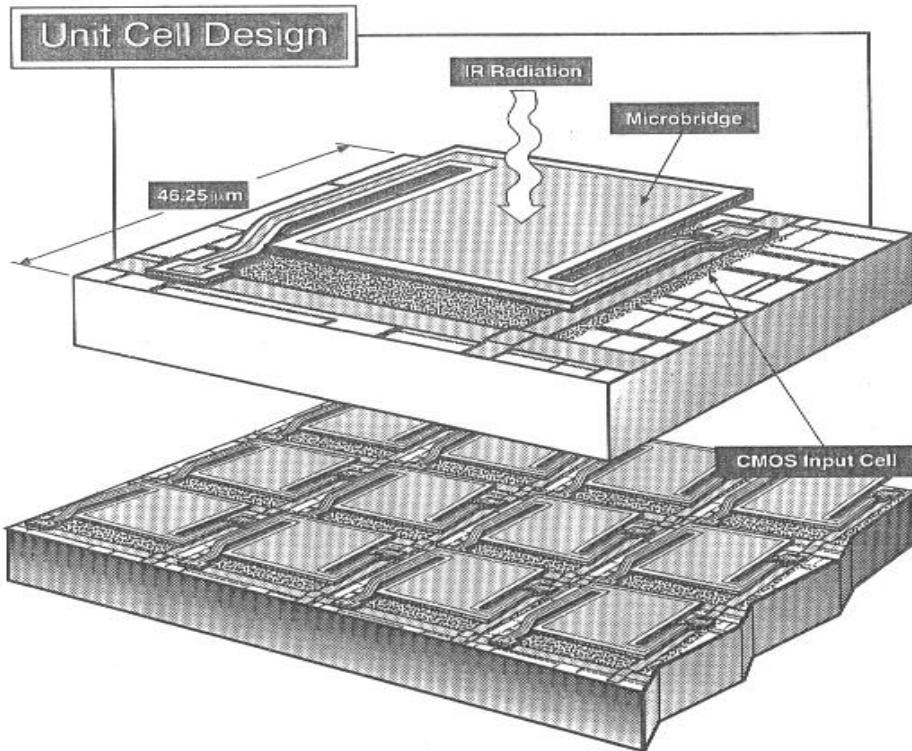
Via-Last Heterogeneous Integration for Piston-Mirrors Using Two-Step Layer Transfer



Lapisa, M., Zimmer, F., Stemme, G., Gehner, A., & Niklaus, F. (2013). Heterogeneous 3D integration of hidden hinge micromirror arrays consisting of two layers of monocrystalline silicon. *Journal of Micromechanics and Microengineering*, 23(7), 075003.

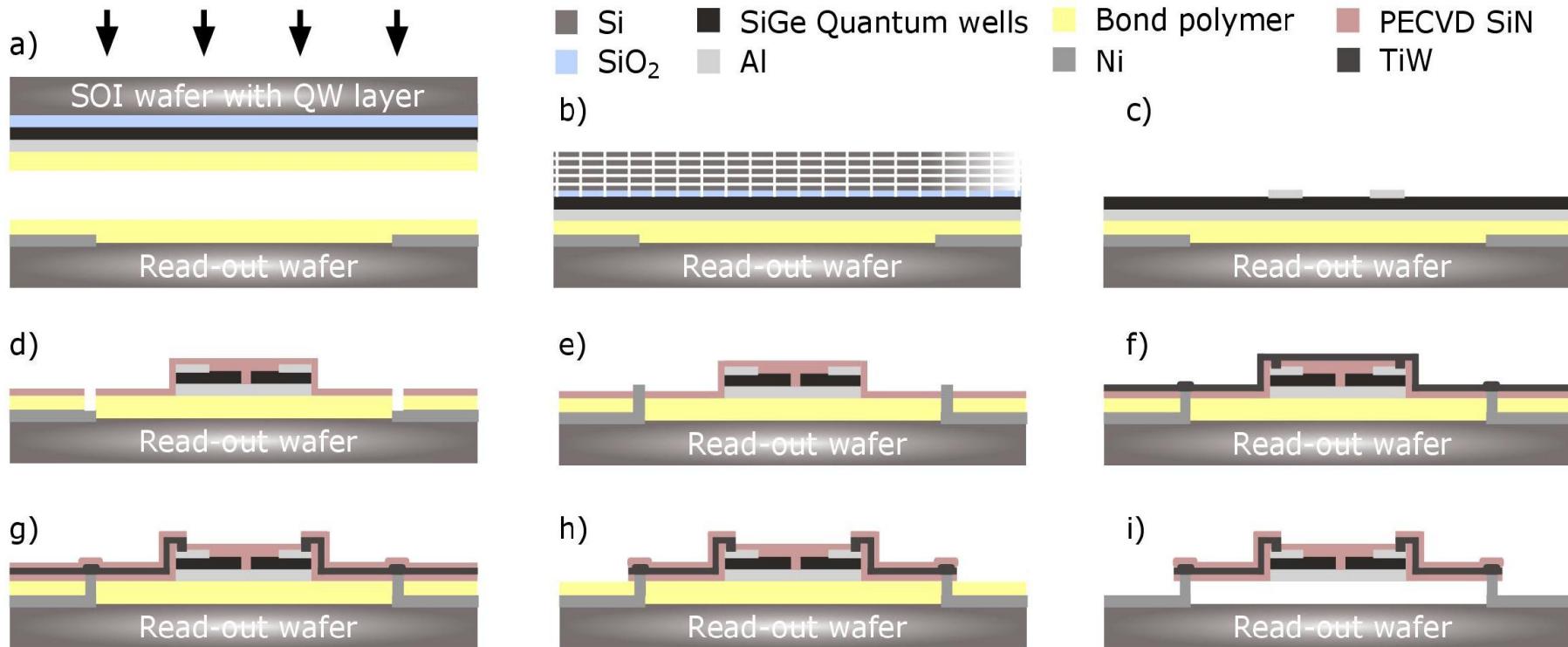


Bolometer Array for IR Imaging

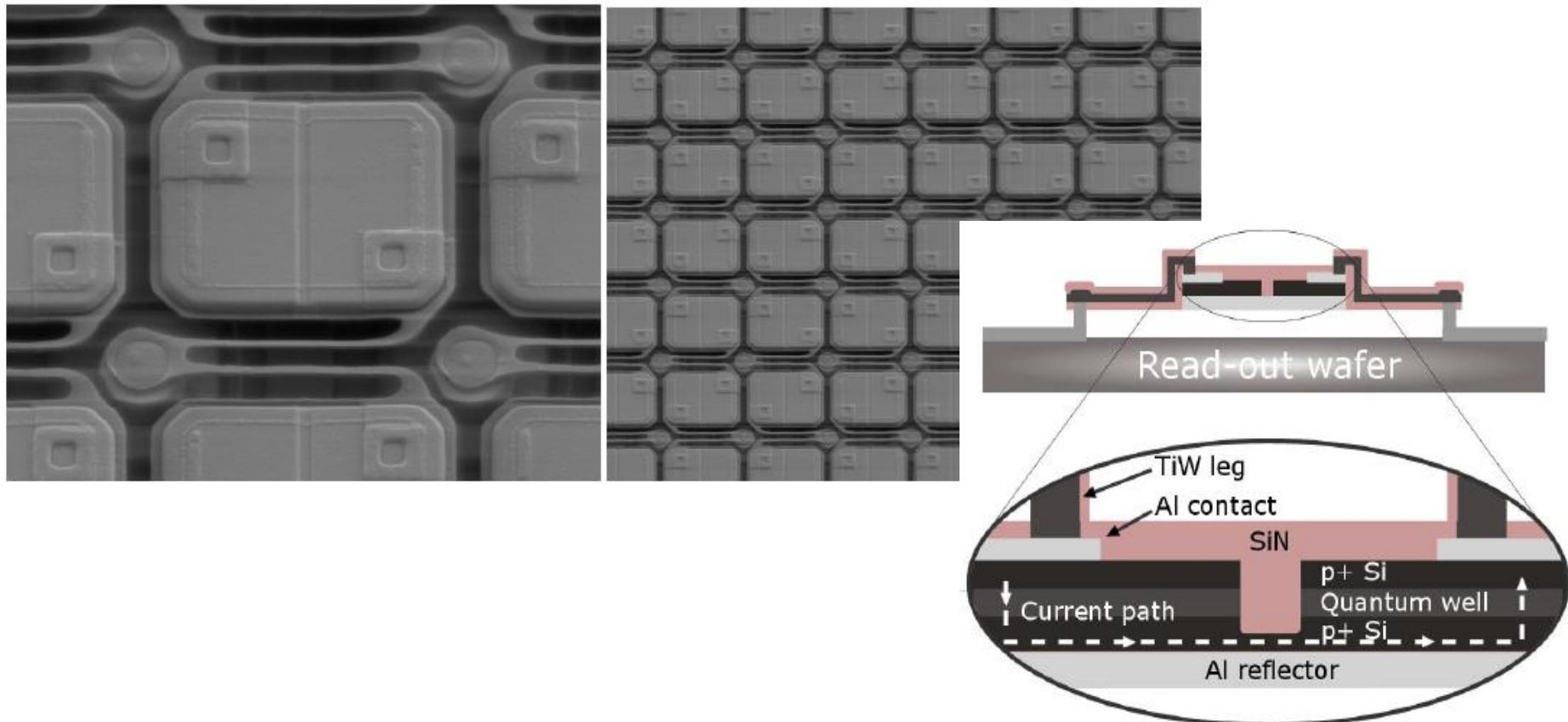


Forsberg, Fredrik, et al. "CMOS-integrated Si/SiGe quantum-well infrared microbolometer focal plane arrays manufactured with very large-scale heterogeneous 3-D integration." *IEEE Journal of Selected Topics in Quantum Electronics* 21.4 (2015): 30-40.

Design of QW Si/SiGe IR Bolometer

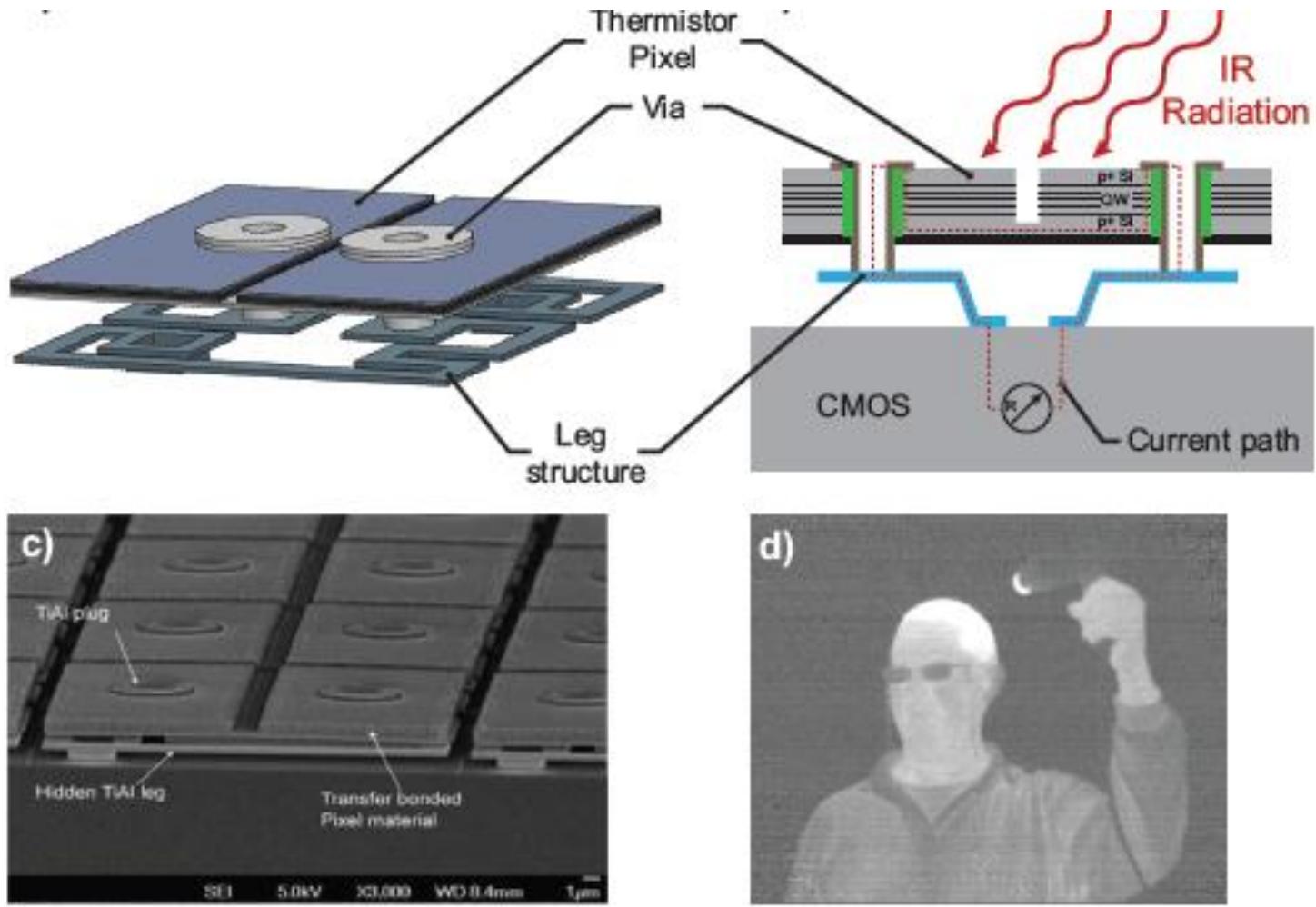


Heterogeneously Integrated 17 μm pitch QW SiGe Bolometers on Fan-Out-Wafers



Forsberg, Fredrik, et al. "CMOS-integrated Si/SiGe quantum-well infrared microbolometer focal plane arrays manufactured with very large-scale heterogeneous 3-D integration." *IEEE Journal of Selected Topics in Quantum Electronics* 21.4 (2015): 30-40.

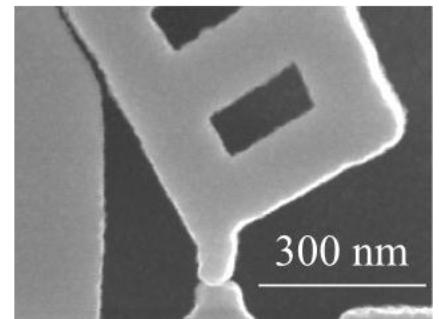
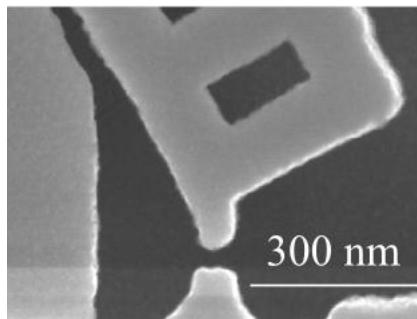
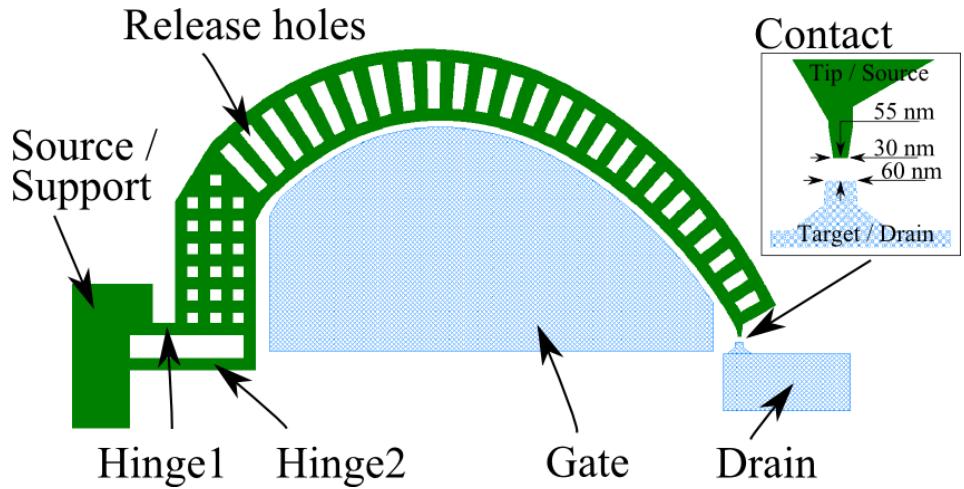
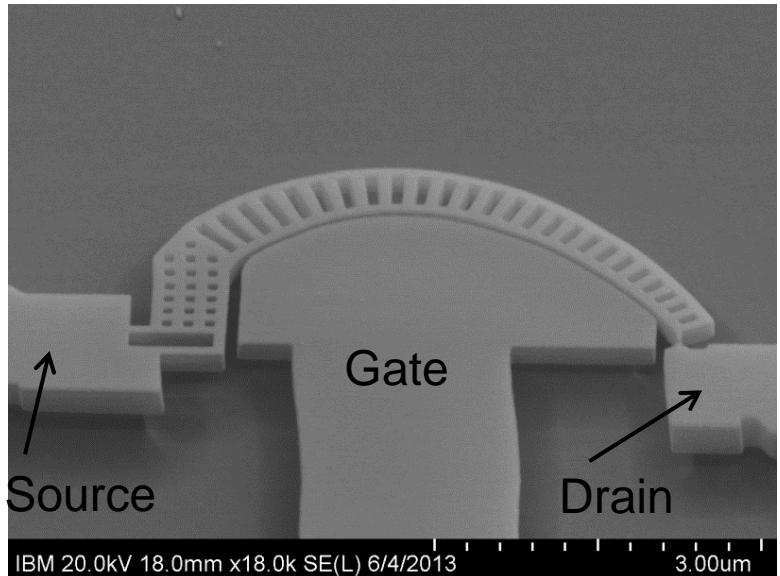
Functional Double-Layer 25 μm pitch IR Bolometers on 0.35 μm CMOS



Forsberg, Fredrik, et al. "CMOS-integrated Si/SiGe quantum-well infrared microbolometer focal plane arrays manufactured with very large-scale heterogeneous 3-D integration." *IEEE Journal of Selected Topics in Quantum Electronics* 21.4 (2015): 30-40.



NEMS Switch Design



erc

IBM

EPFL
ÉCOLE POLYTECHNIQUE
FÉDÉRALE DE LAUSANNE

University of
BRISTOL

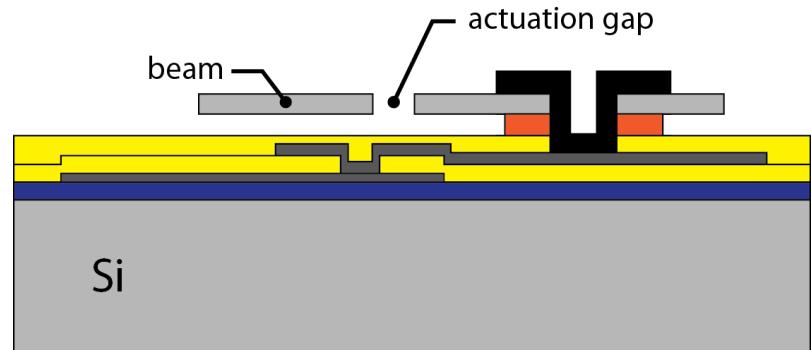
ST

LANCASTER
UNIVERSITY

Integration of NEM Switches

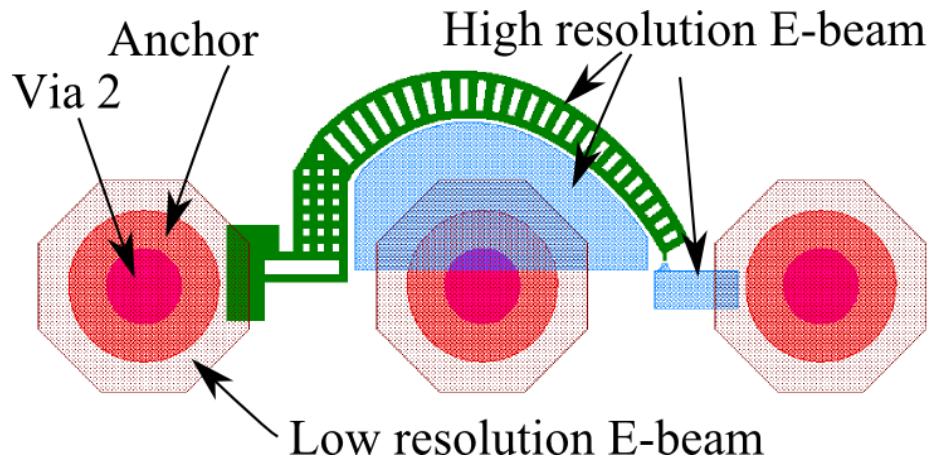
Goal:

NEM switch on top of 2 metal layer interconnect wafer

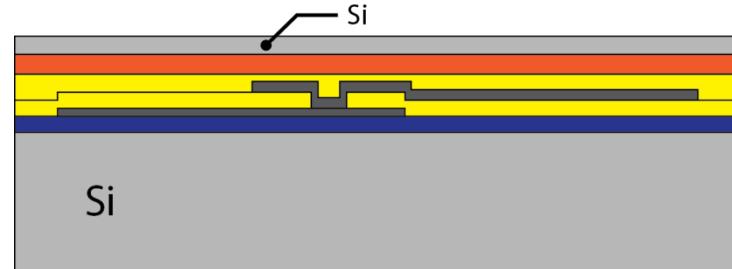
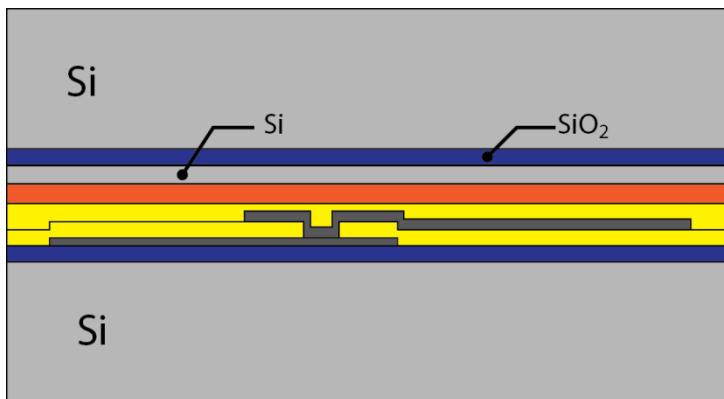
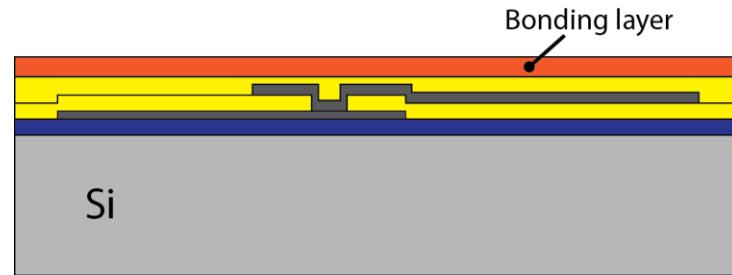
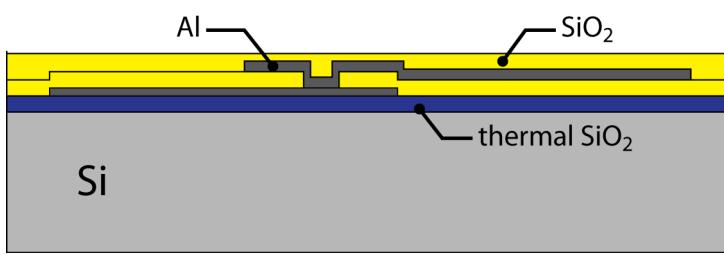


Method:

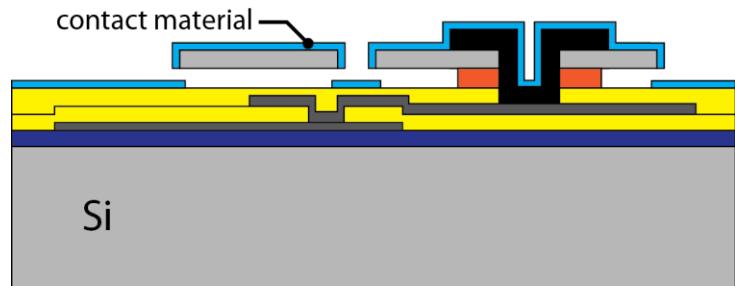
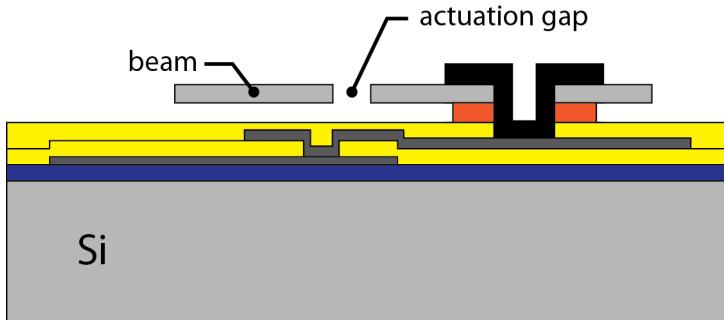
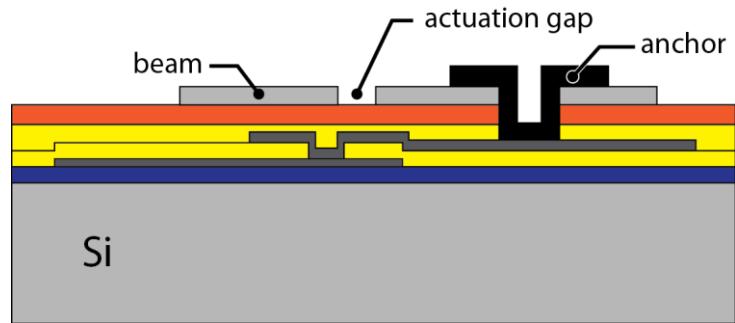
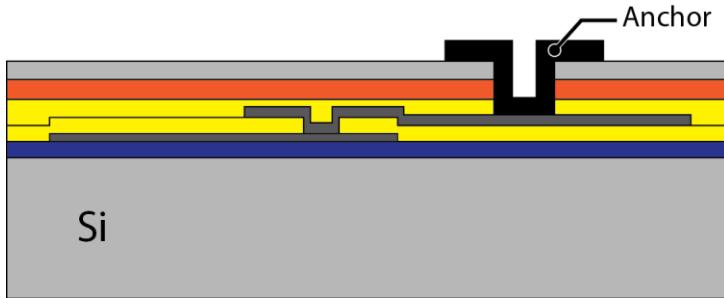
Metal anchors for mechanical stability and electrical connection



Heterogeneous Integration Process



Heterogeneous Integration Process

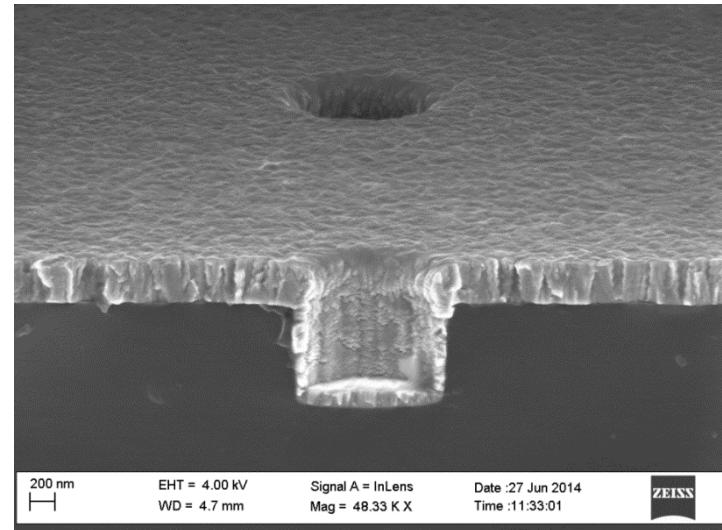
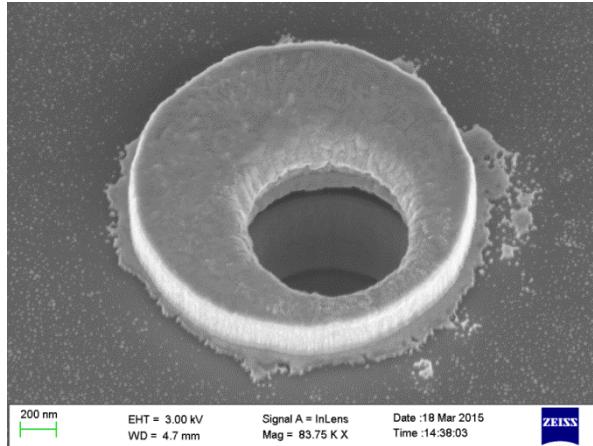
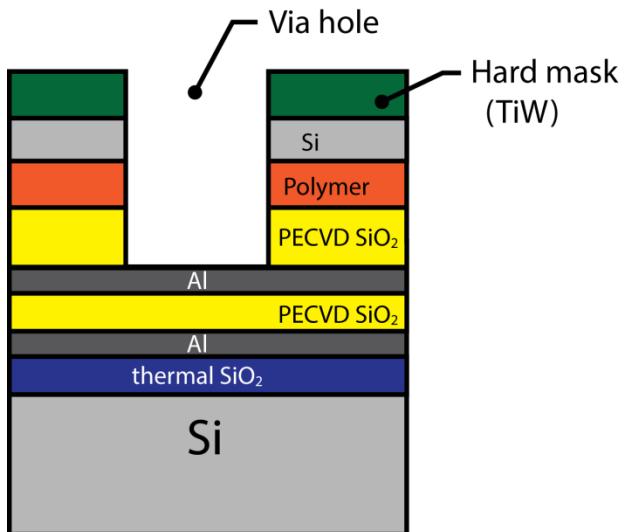


Challenges

Etching of Anchor holes

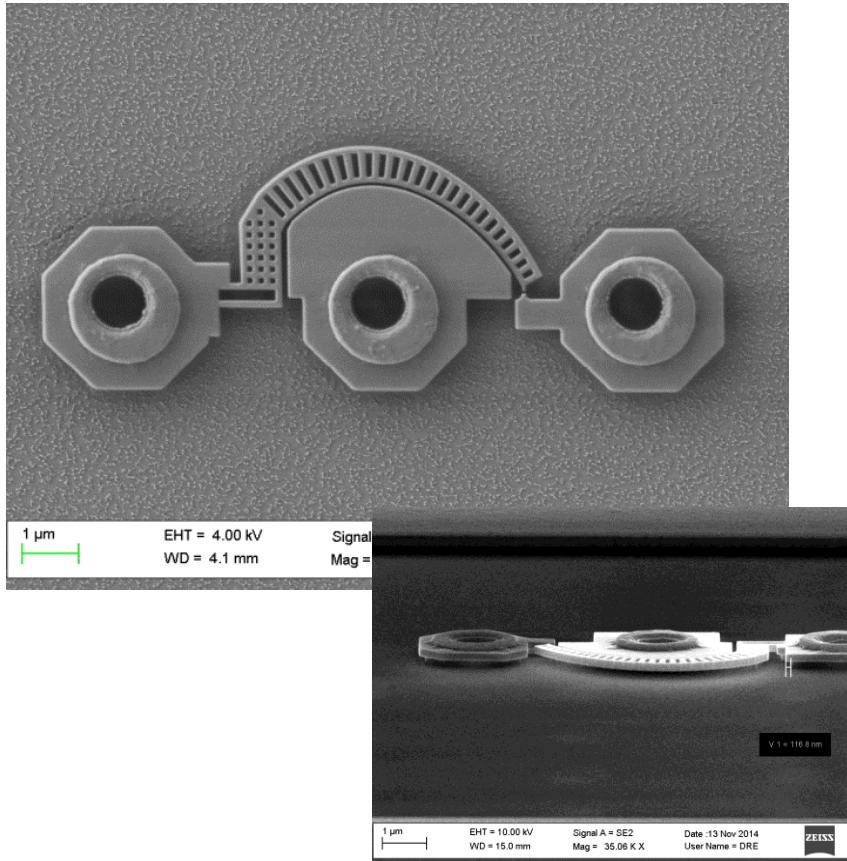
- Use hard mask to etch through different materials

→ How do you know when to stop etching?





Integrated Moni-Si NEM Switches

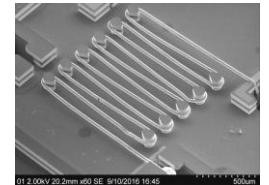


Qin, T., Bleiker, S. J., Rana, S., Niklaus, F., & Pamunuwa, D. (2018). Performance Analysis of Nanoelectromechanical Relay-Based Field-Programmable Gate Arrays. *IEEE Access*.

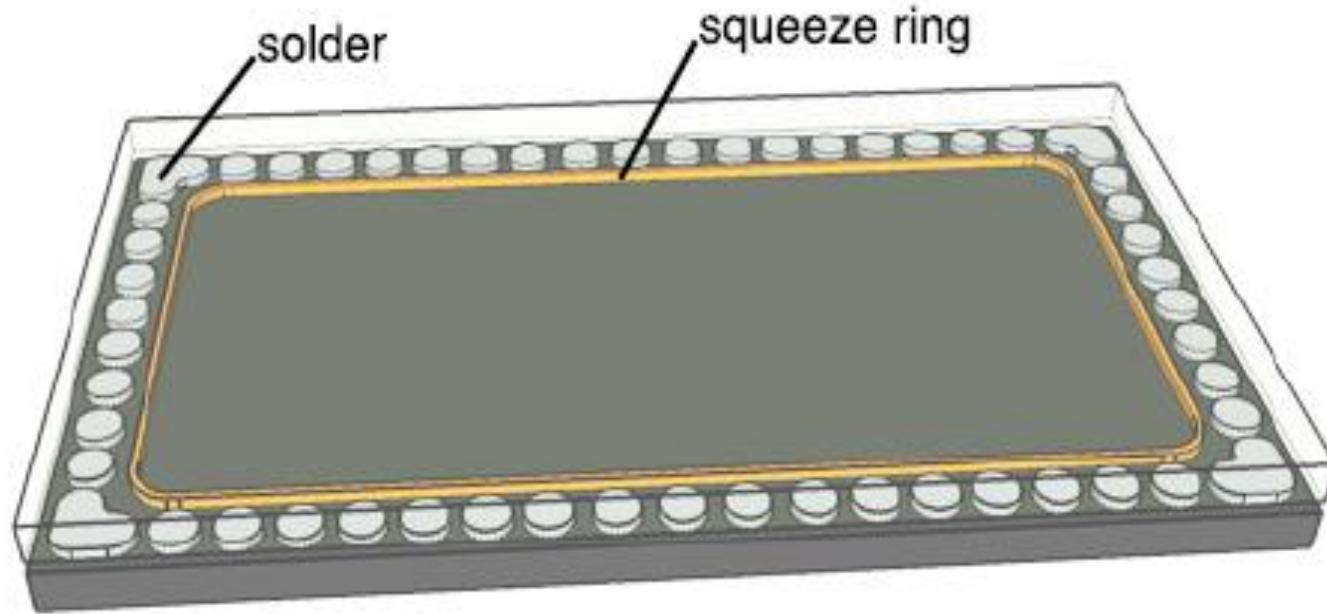


Research Topics in Group

- Heterogeneous 3D Integration for MEMS & NEMS
- **Integration and Packaging for MEMS**
- Nanomanufacturing Technologies and Graphene NEMS

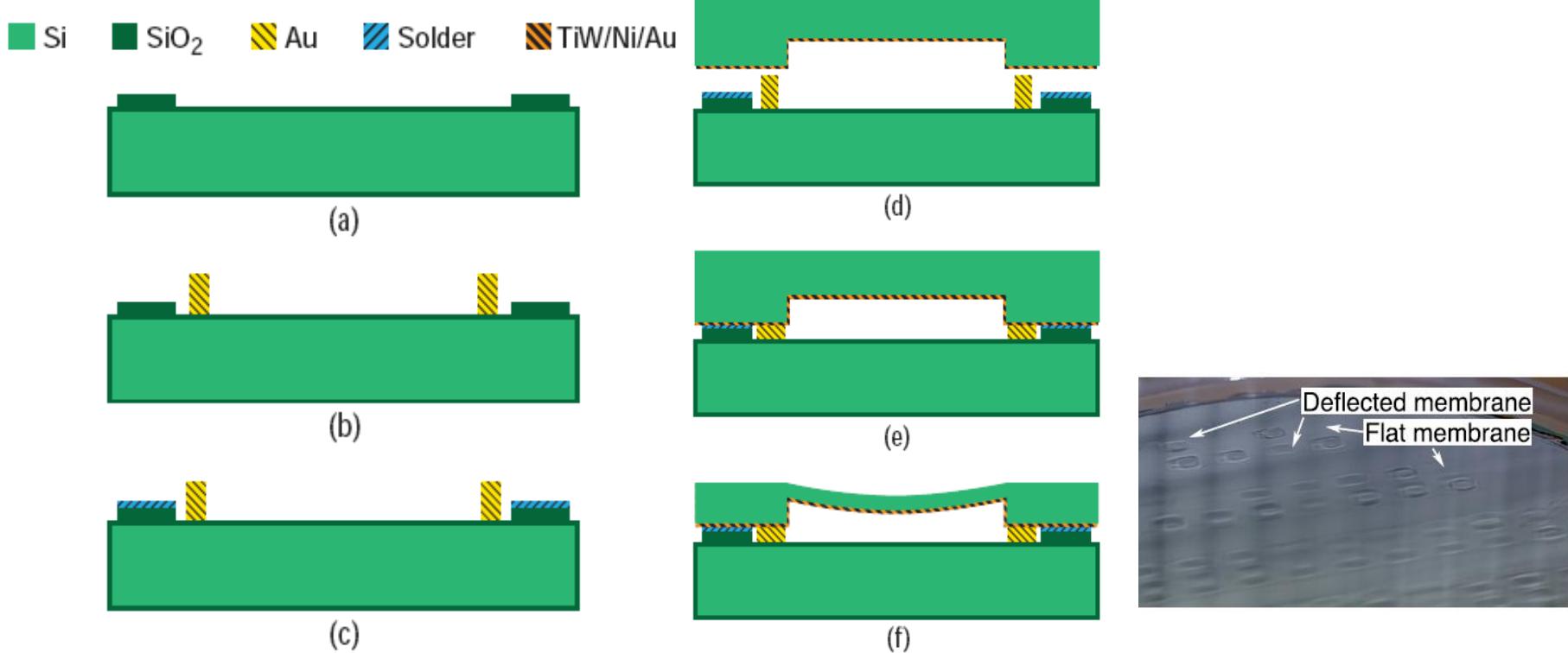


Wafer-Level Vacuum Sealing Using Cold Metal Welding in Combination with Solder Bumps



- Au sealing ring prevents solder vapor from entering cavity.
- Solder bumps provide bond strength.

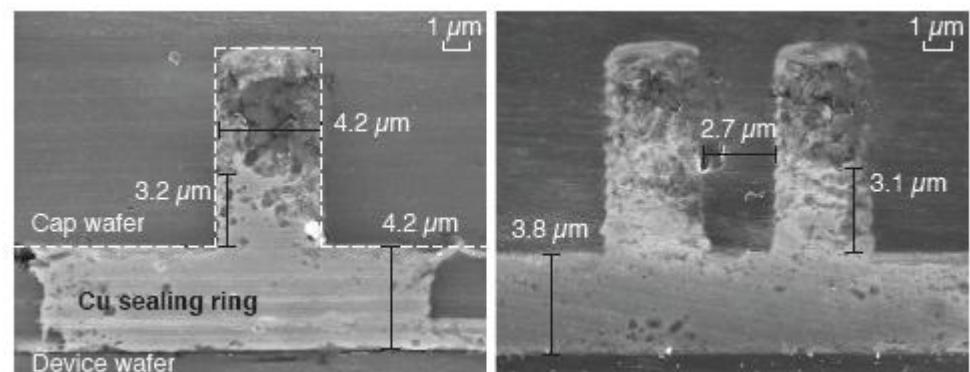
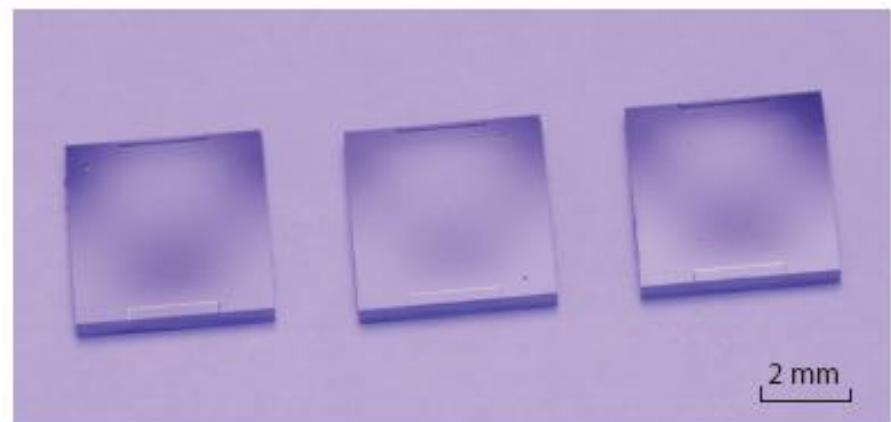
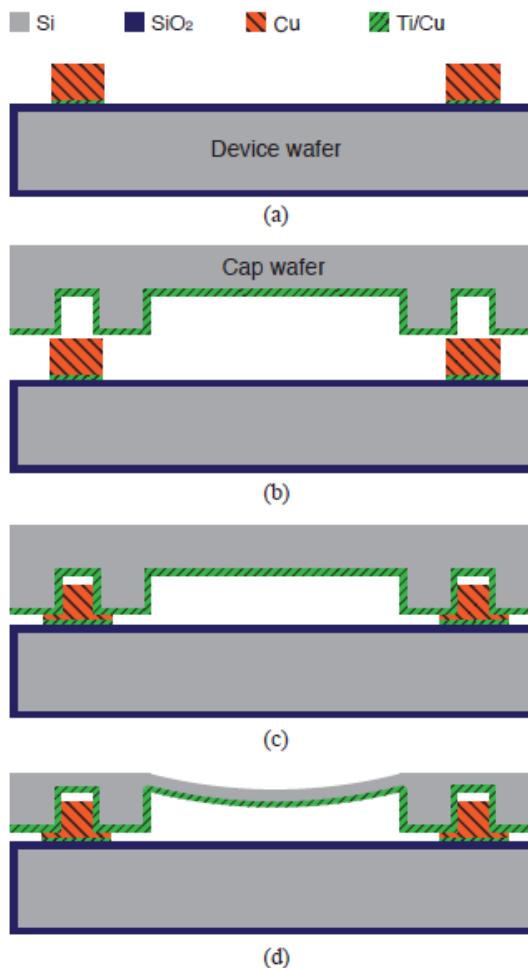
Wafer-Level Vacuum Sealing: Process Flow



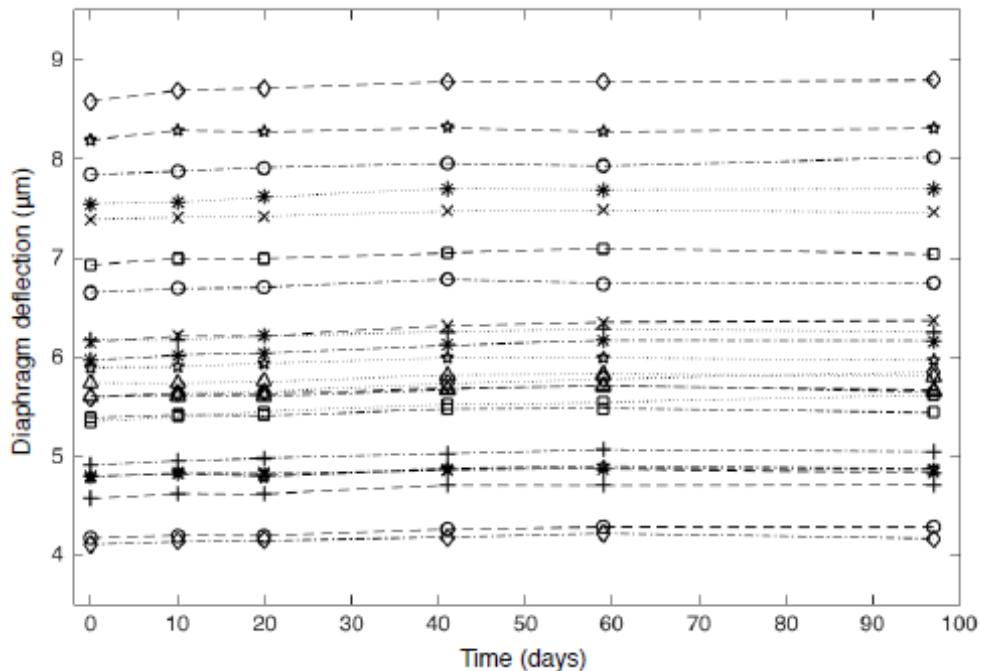
Antelius, M., Stemme, G., & Niklaus, F. (2011). Small footprint wafer-level vacuum packaging using compressible gold sealing rings. *Journal of Micromechanics and Microengineering*, 21(8), 085011.



Wafer-Level Low-Temperature Vacuum Sealing Using 8 μm Wide Copper Rings



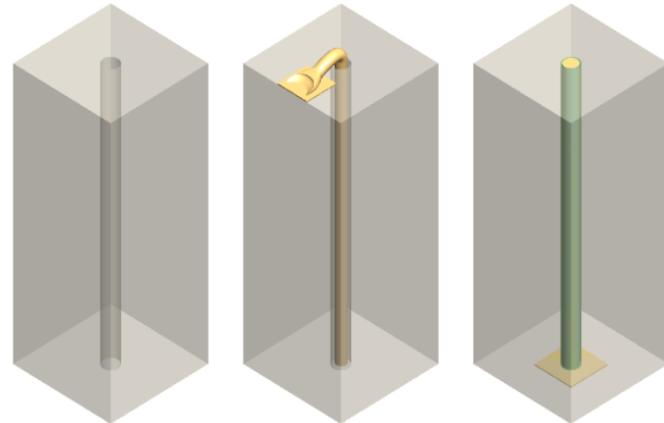
Wafer-Level Low-Temperature Vacuum Sealing Using Copper Sealing



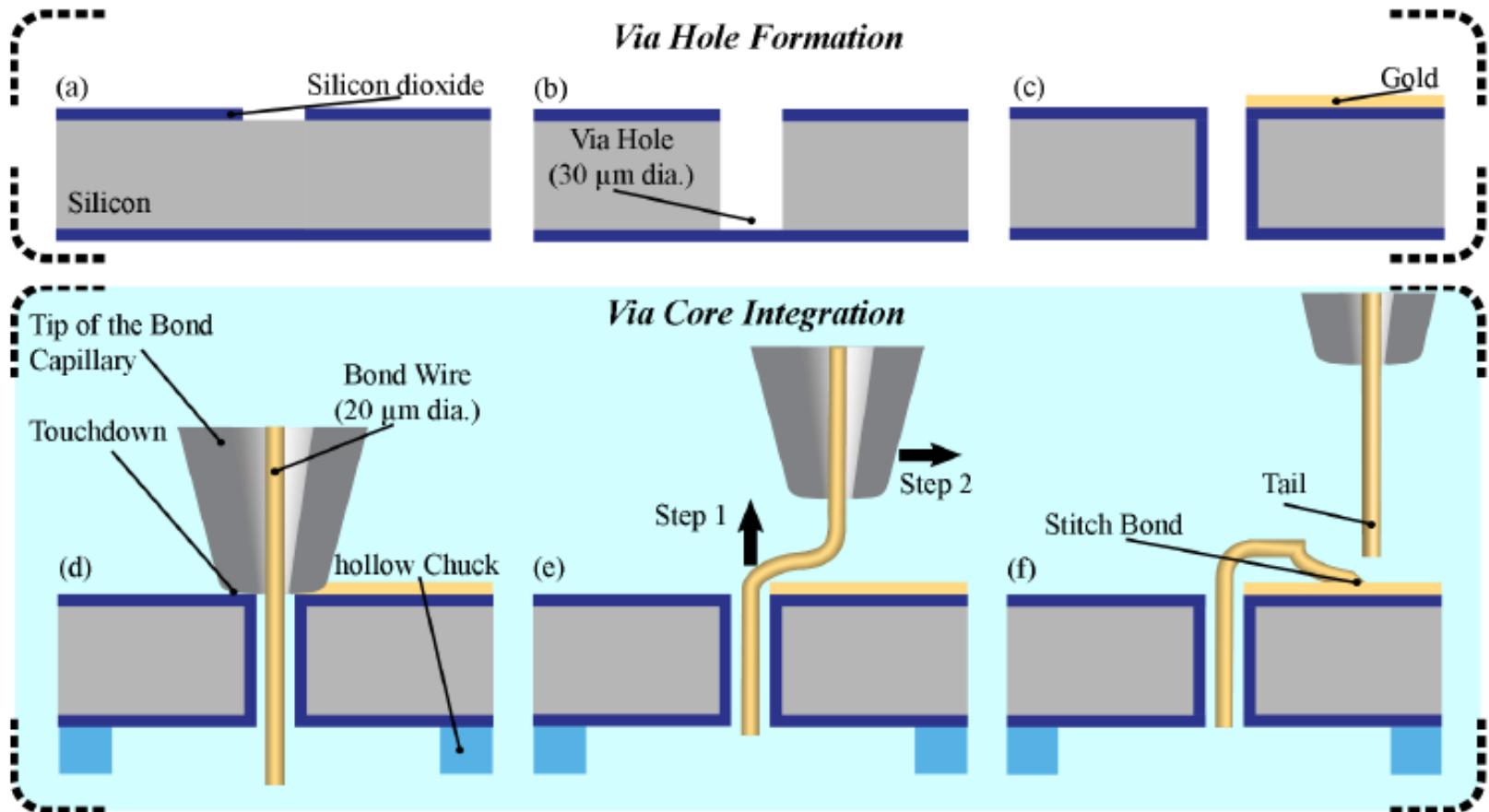
Gas	O2G2 design		O2G3 design	
	Pressure (mbar)	Percent (%)	Pressure (mbar)	Percent (%)
H ₂	2.9×10^{-2}	63.07	0	0
CO ₂	1.1×10^{-2}	23.92	0	0
CO	5.1×10^{-3}	11.09	0	0
CH ₄	0	0	2.5×10^{-2}	97.66
CHs ^a	6.7×10^{-4}	1.46	4.5×10^{-4}	1.76
Ar	2.1×10^{-4}	0.46	1.3×10^{-4}	0.51
He	0	0	1.8×10^{-5}	0.07
O ₂	0	0	0	0
N ₂	0	0	0	0
H ₂ O	0	0	0	0
Total	4.6×10^{-2}	100.00	2.6×10^{-2}	100.00

Wire Bonded TSVs

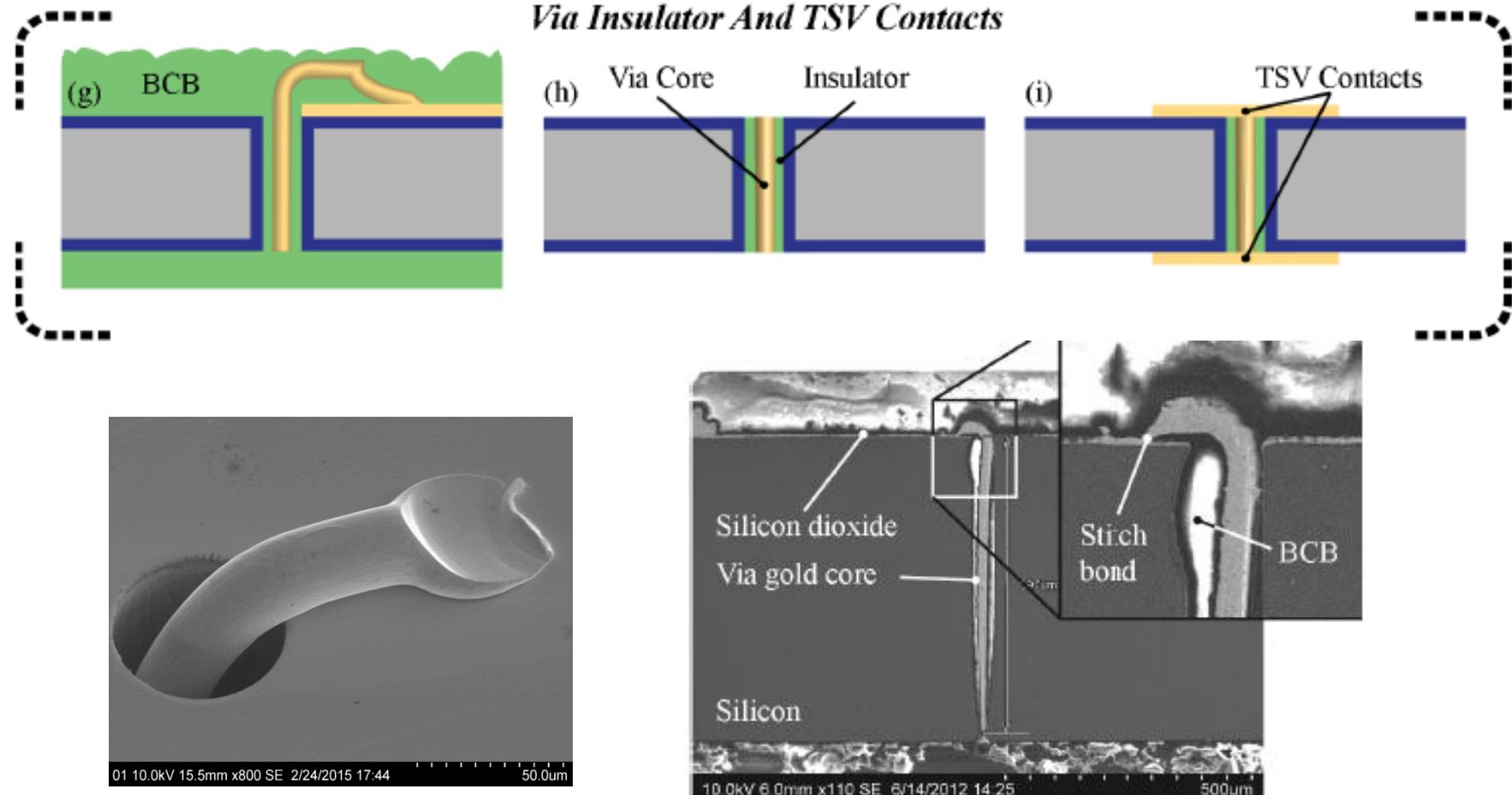
- Low-cost for low to medium TSV density
- Enable high aspect ratio TSV formation
- No lithography (mask-less) TSV formation
- Low temperature budget approach



TSVs Manufacturing Using Wire Bonding

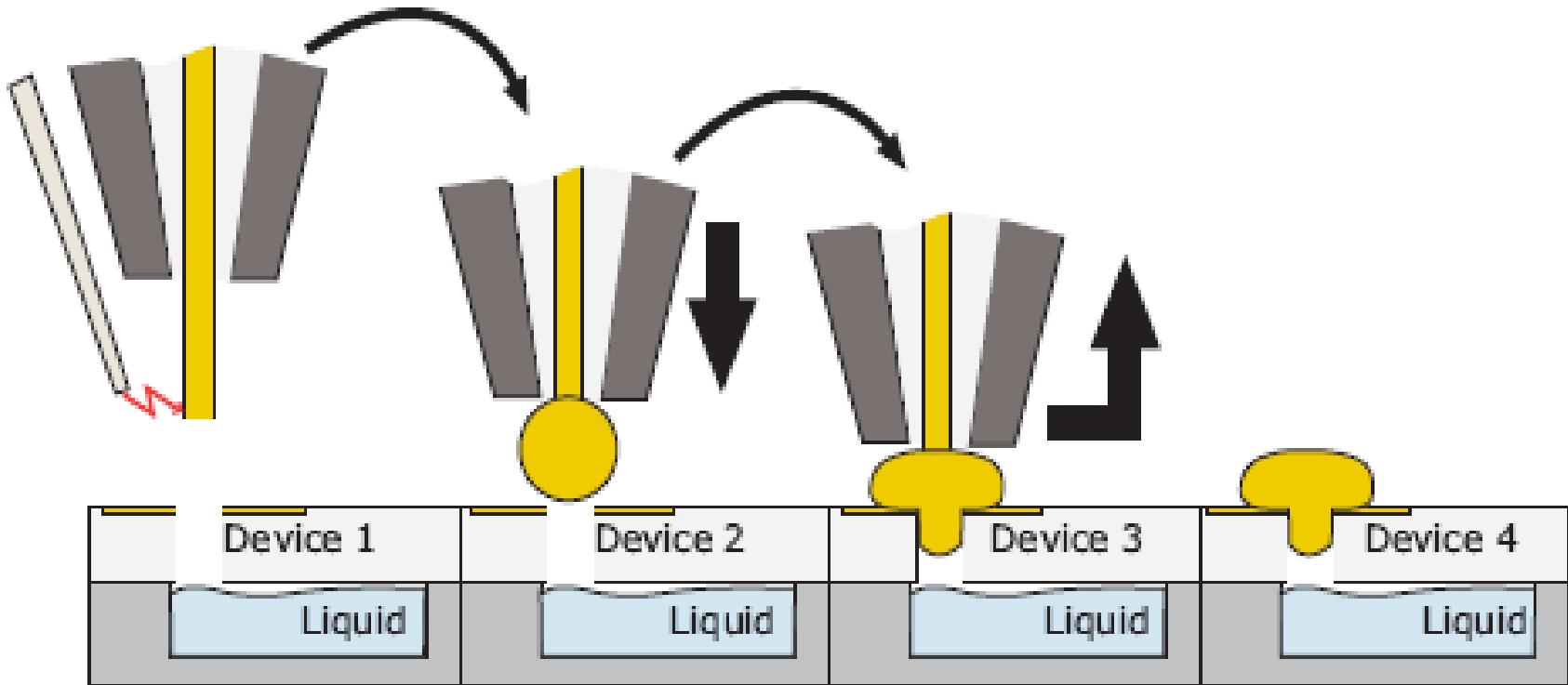


Gold TSVs with Aspect Ratios > 20



Schröder, Stephan, et al. "Very high aspect ratio through silicon vias (TSVs) using wire bonding." *Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS & EUROSENSORS XXVII)*, 2013 Transducers & Eurosensors XXVII: The 17th International Conference on. IEEE, 2013.

Sealing of Liquids in MEMS Cavities Using Cold Metal Plugging



Sealing of Liquids in MEMS Cavities Using Cold Metal Plugging

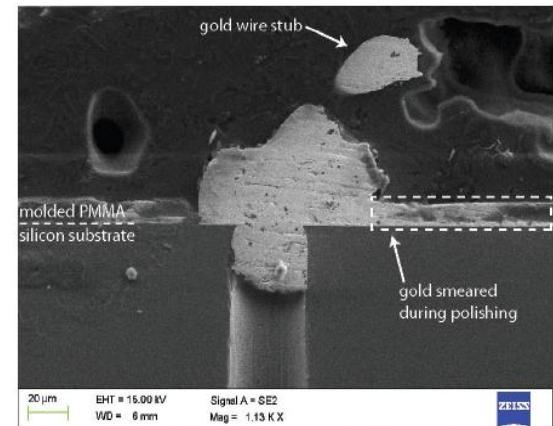
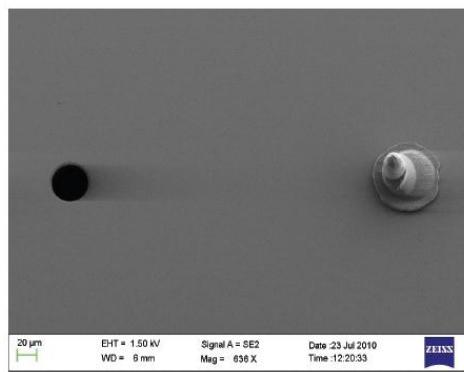
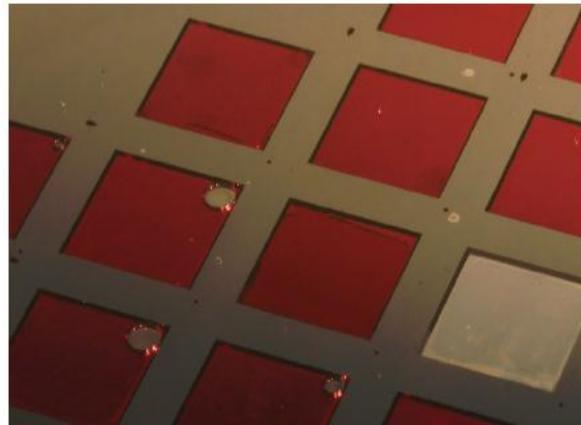
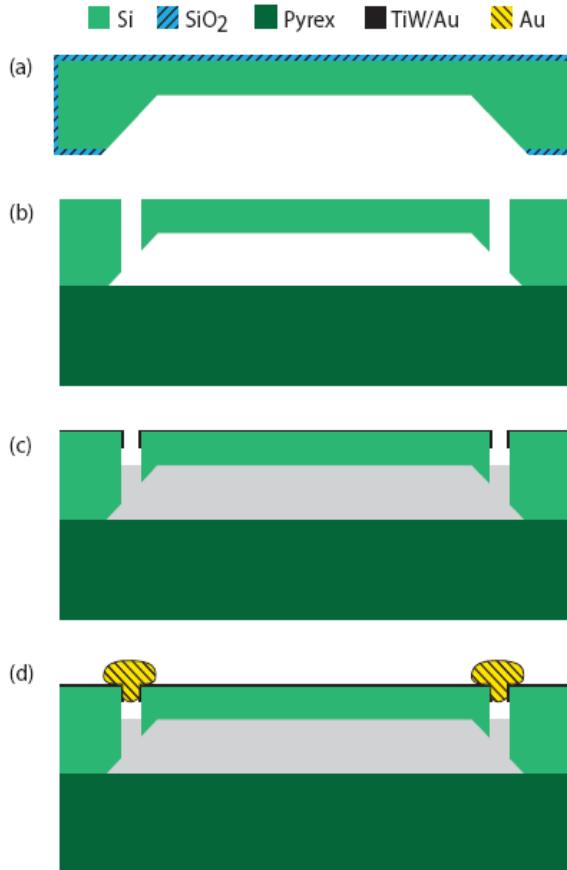
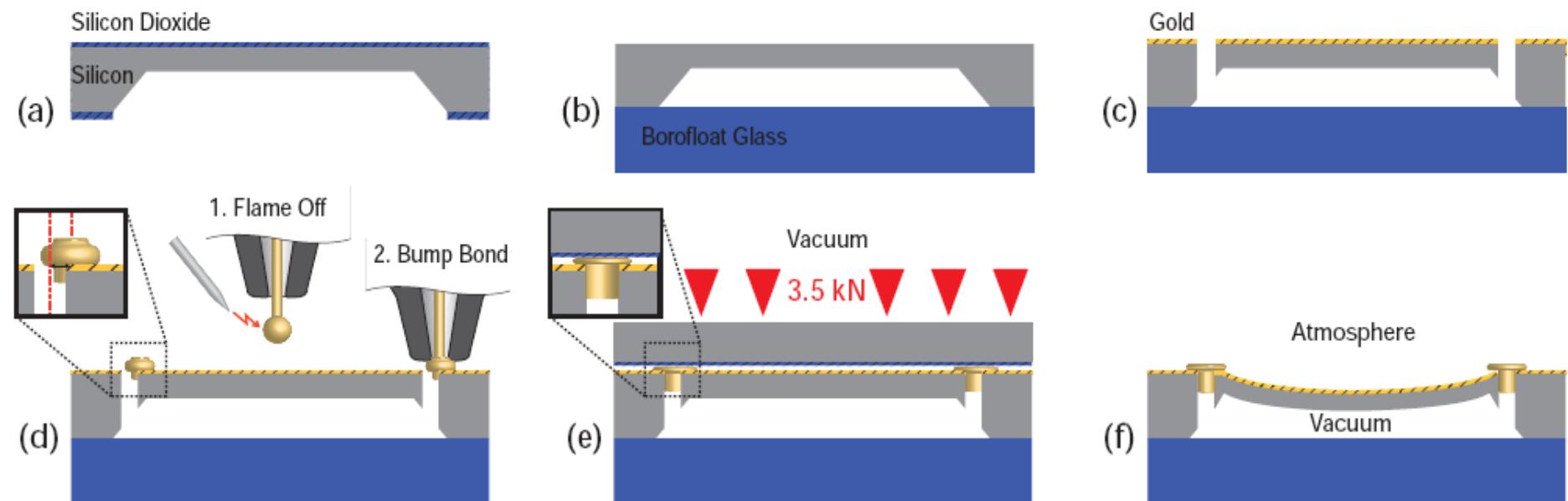
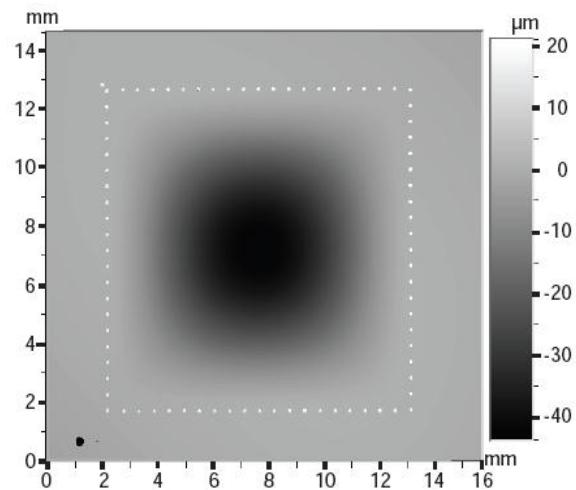
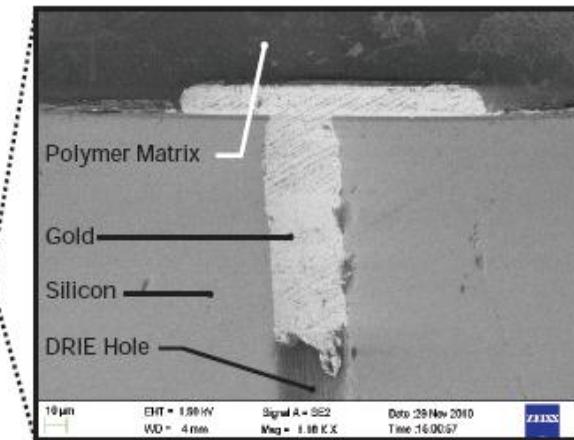
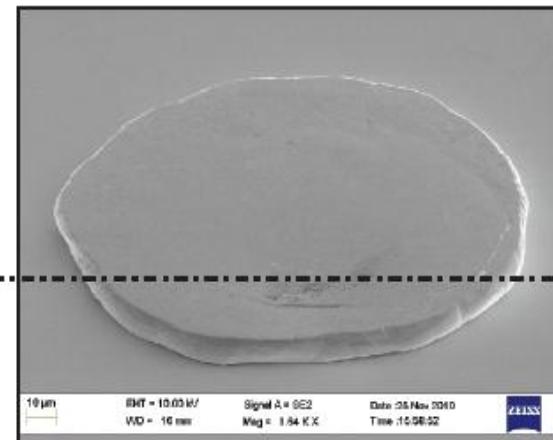
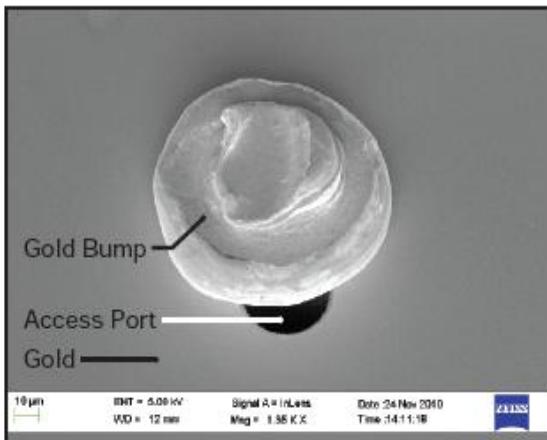


Image source: Antelius, Proc Transducers 2011, KTH

Wafer-Level Vacuum Sealing Using Cold Metal Plugging



Wafer-Level Vacuum Sealing Using Cold Metal Plugging

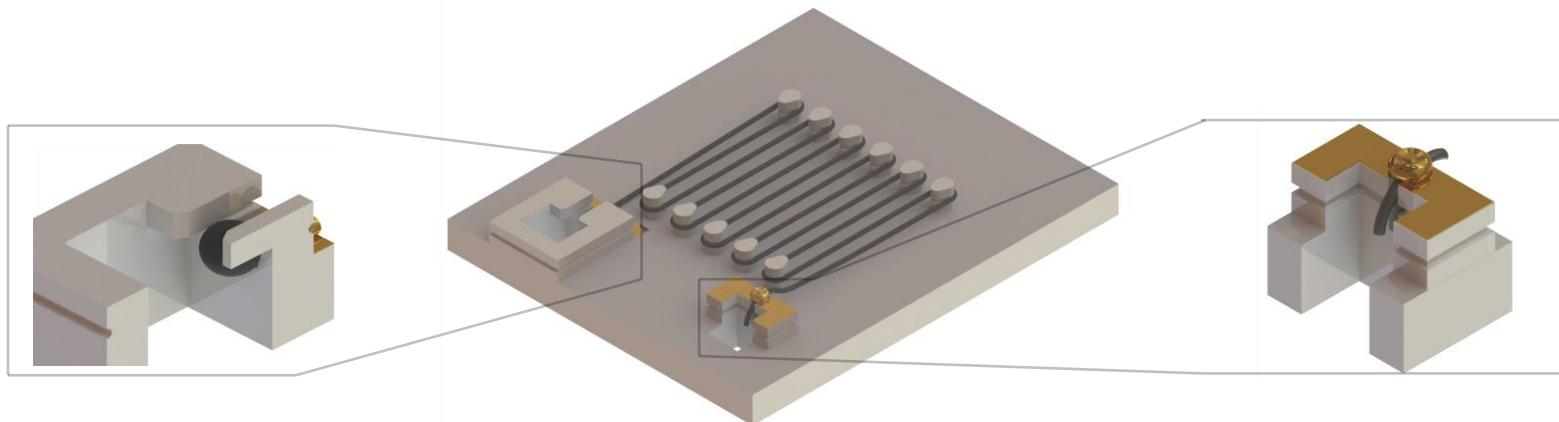


Gas	Pressure, 2 ports		Pressure, 80 ports	
	[mbar]	%	[mbar]	%
H ₂ O	3.33×10^{-3}	56.96 ^a	0	0
Ar	1.00×10^{-3}	17.17	6.15×10^{-4}	75.11
N ₂	8.52×10^{-4}	14.56	0	0
H ₂	5.25×10^{-4}	8.97	0	0
CH ₄	8.75×10^{-5}	1.50	0	0
O ₂	2.77×10^{-5}	0.47	0	0
CO ₂	2.18×10^{-5}	0.37	2.04×10^{-4}	24.86
He	0	0	1.89×10^{-7}	0.02
Ne	0	0	0	0
C ₂ H ₆	0	0	0	0
C ₃ H ₈	0	0	0	0
CO	0	0	0	0
Kr	0	0	0	0
Total	5.85×10^{-3}	100.00	8.19×10^{-4}	100.00

Image source: Antelius, Proc Transducers 2011, KTH

Wire Bonded Infrared Emitter

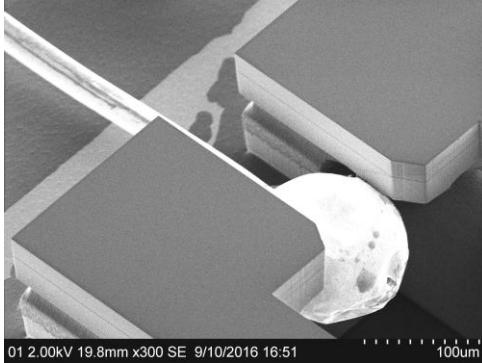
- Joule-heated suspended Kanthal filament
- Integration using an automated wire bonding tool
- Mechanical fixation and placement by
 - Attachment structures for free air ball & wire
 - Guiding posts



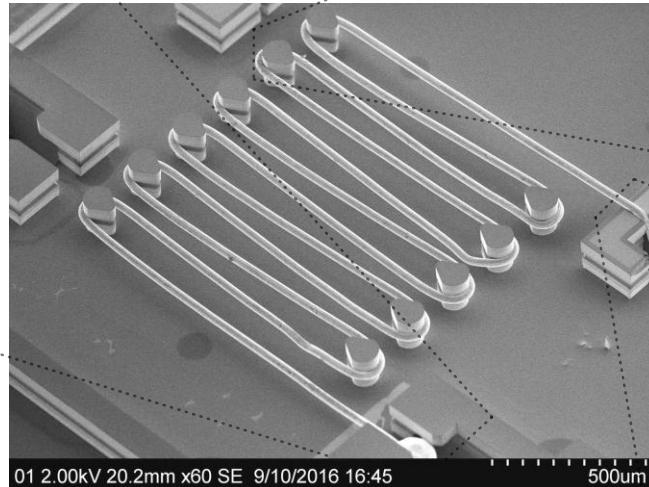
Schröder, Stephan, et al. "Fabrication of an infrared emitter using a generic integration platform based on wire bonding." *Journal of Micromechanics and Microengineering* 26.11 (2016): 115010.

Filament Integration Results

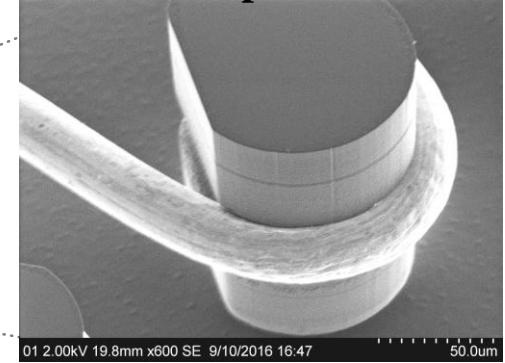
2. Free air ball attachment



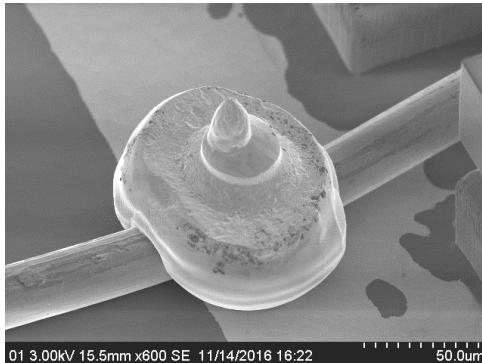
1. Filament Emitter



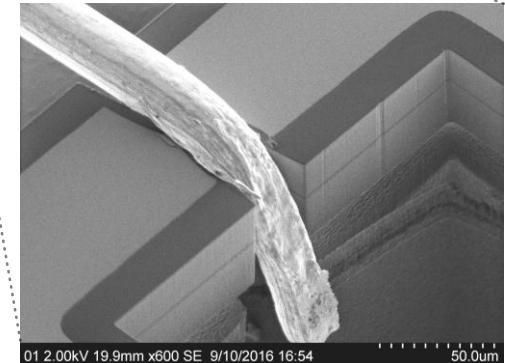
3. Filament placement



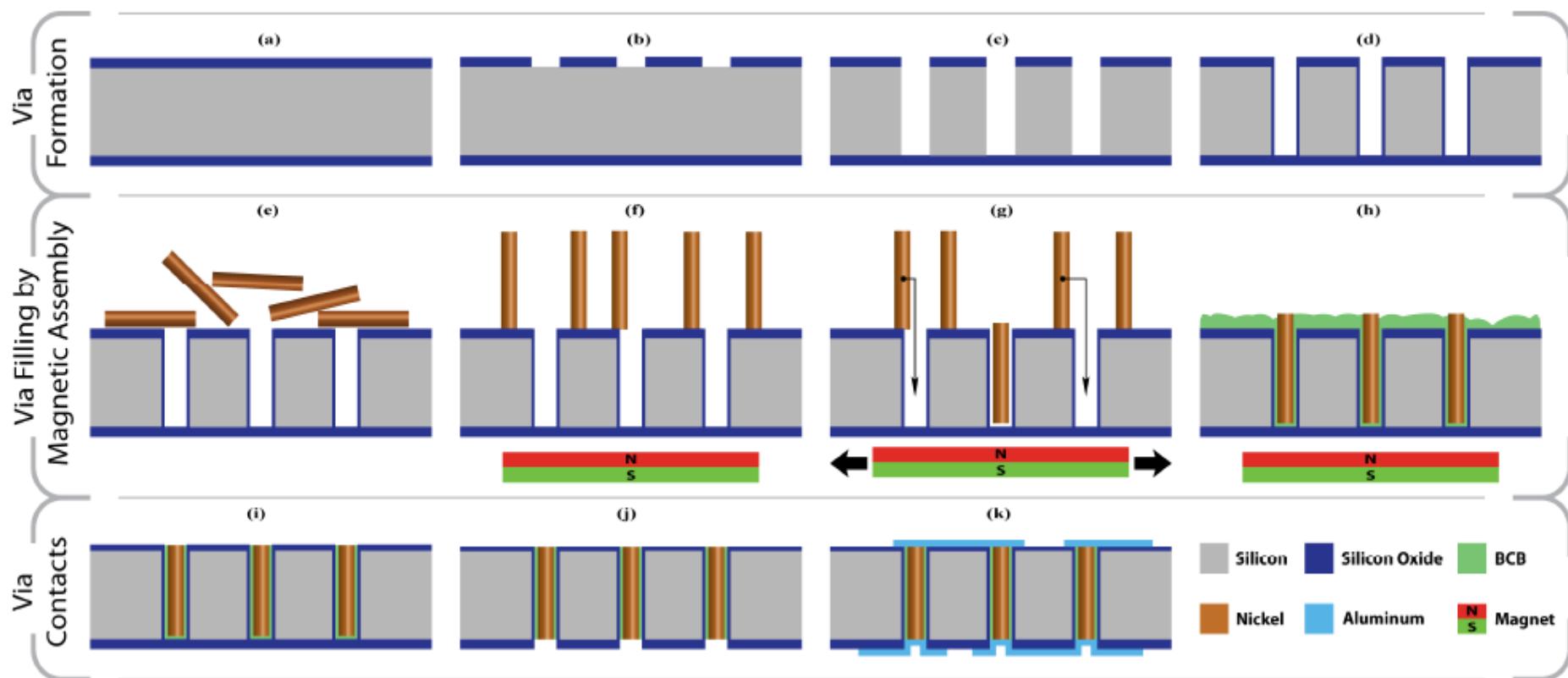
5. Electrical contact



4. Filament attachment



Fabrication of High-Aspect Ratio TSVs by Magnetic Assembly of Metal Studs





High-Aspect Ratio Nickel TSVs

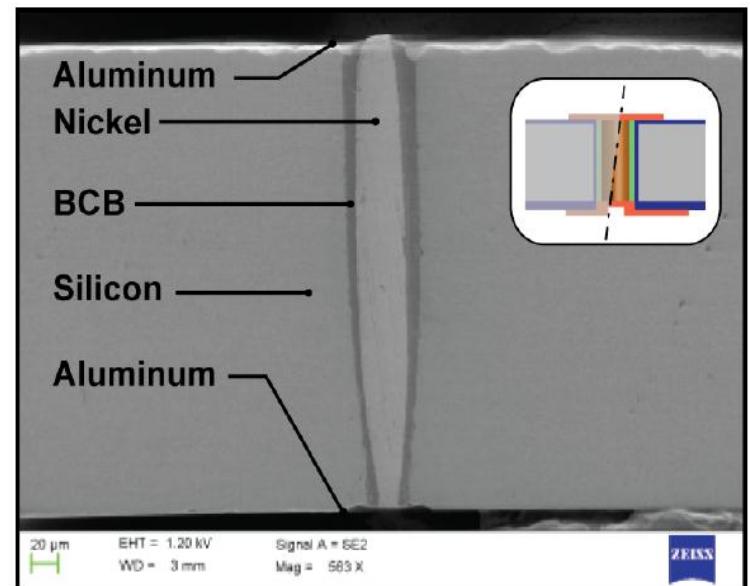
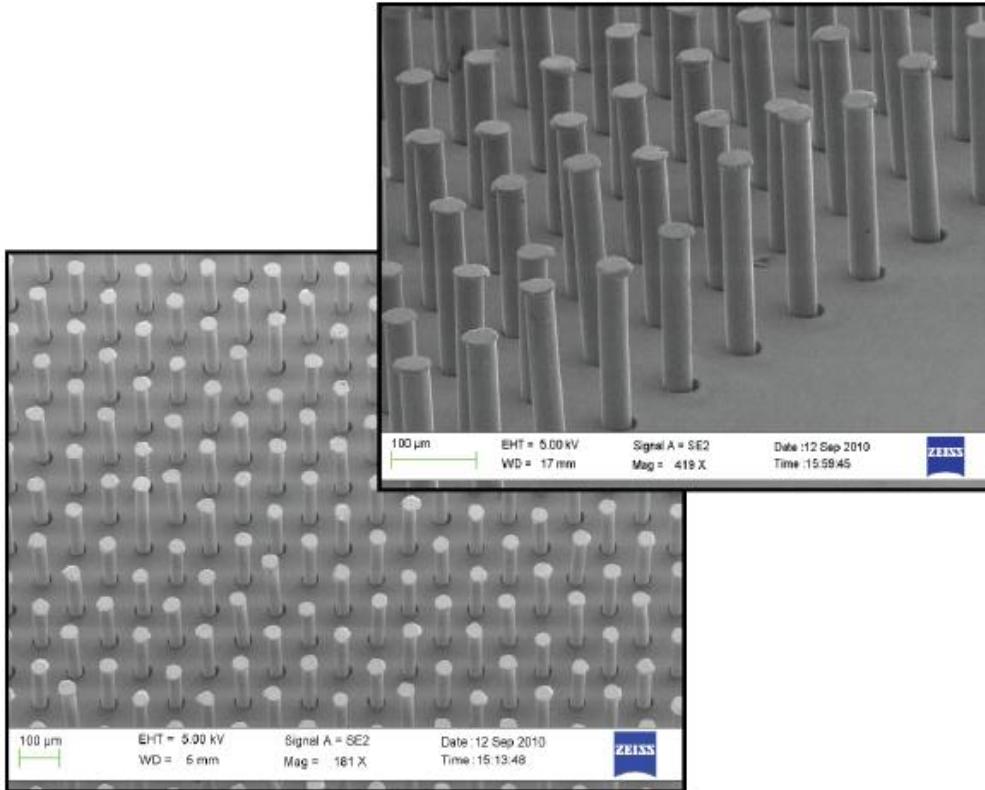


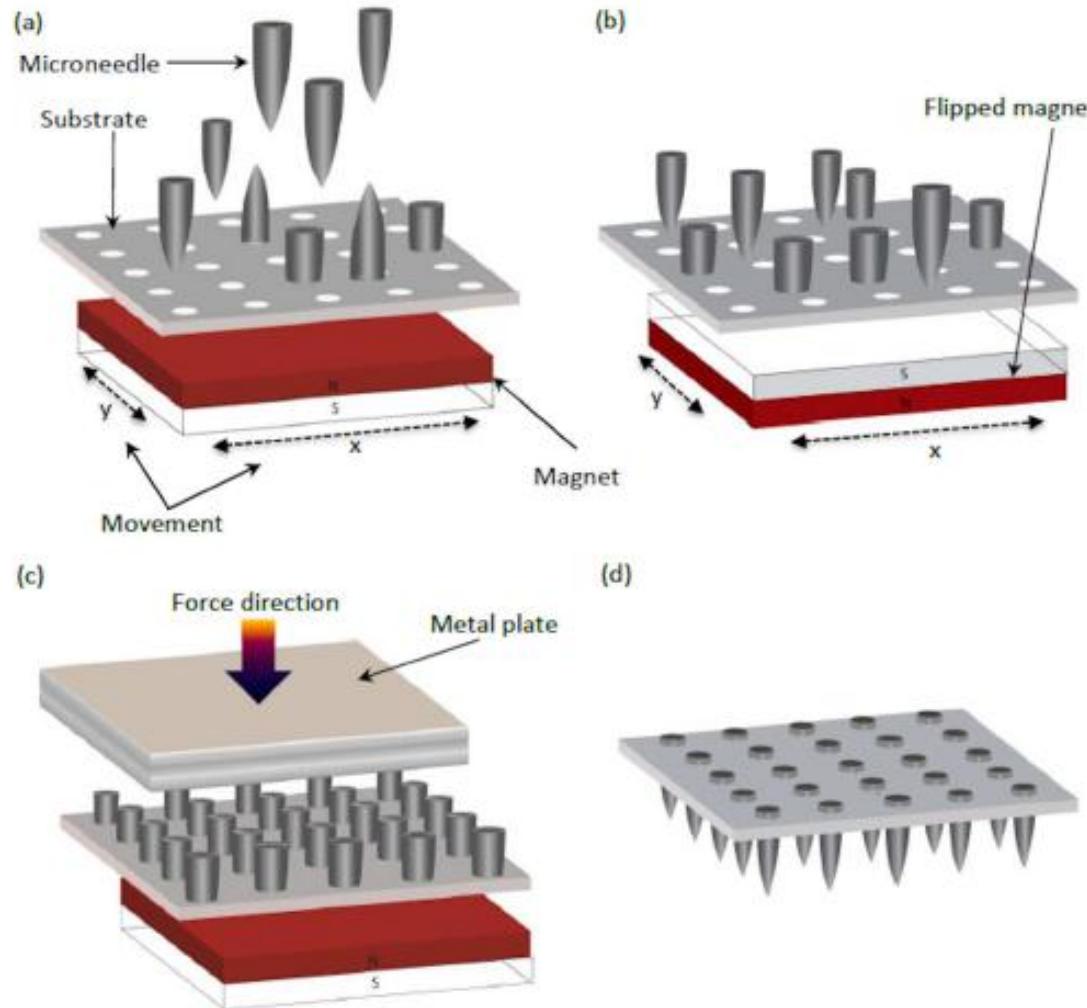
Image source: Fischer, Proc MEMS 2011, KTH



Robotic Magnetic Self-assembly of TSVs

Image source: Fischer, Proc MEMS 2011, KTH

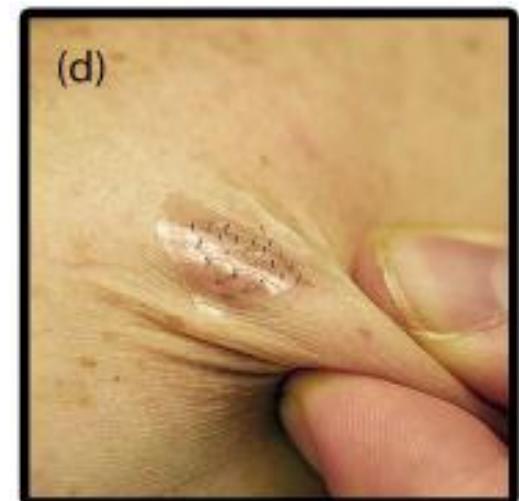
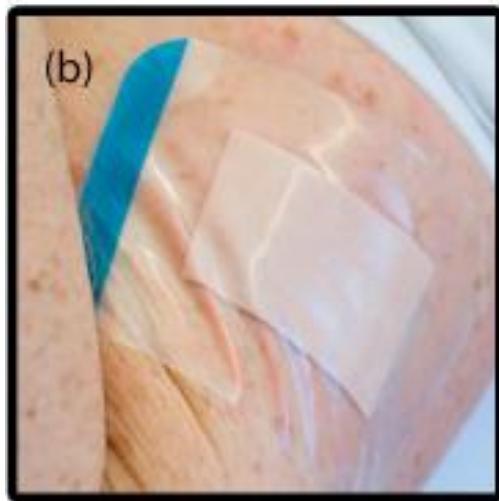
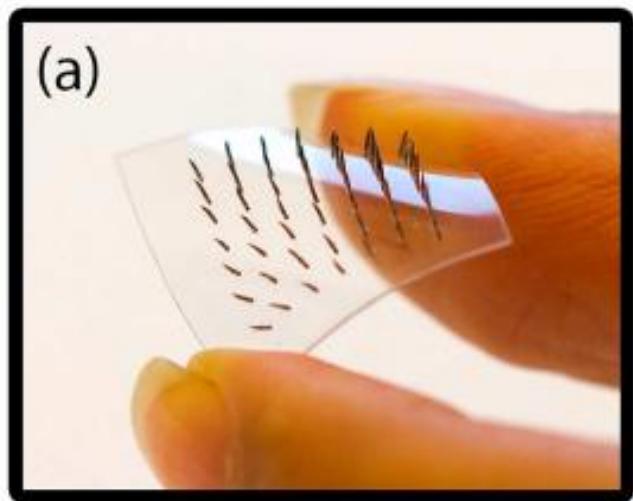
Magnetic Self-assembly for Stretchable Microneedle Patches



Magnetic Self-assembly for Stretchable Microneedle Patches

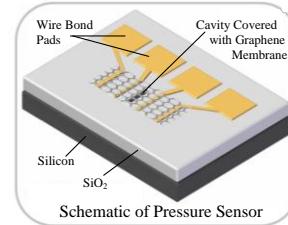
Combination of :

**Stretchable and flexible substrate for comfort; and
Sharp and stiff needles for reliable penetration**

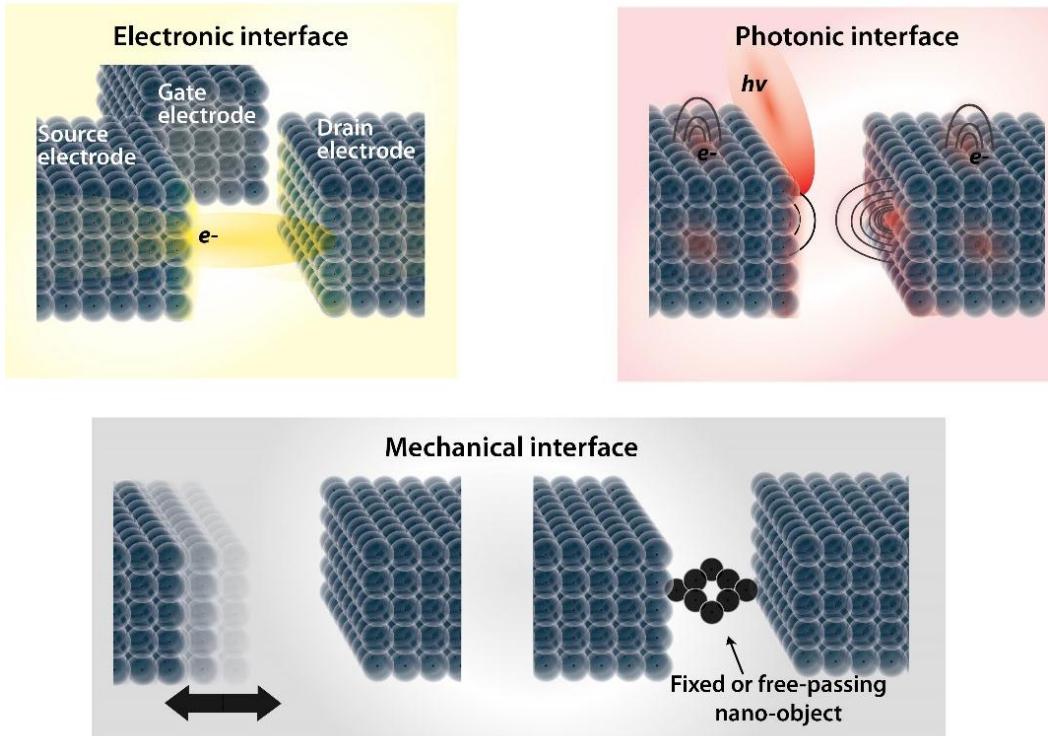


Research Topics in Group

- Heterogeneous 3D Integration for MEMS & NEMS
- Integration and Packaging for MEMS
- Nanomanufacturing Technologies and Graphene NEMS



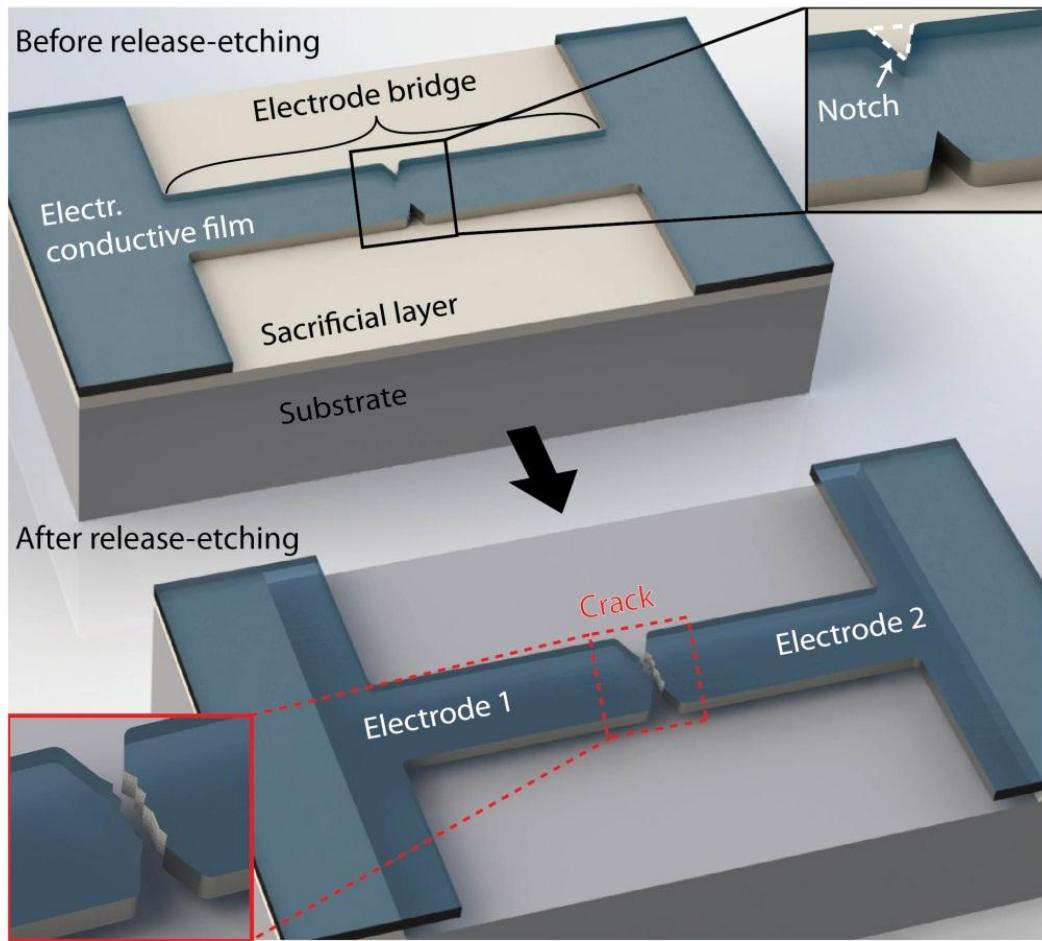
Nanogap Electrodes



Nanogap electronics:
Require sub-3 nm wide gaps between electrodes !

Major problem: Extremely difficult to realize

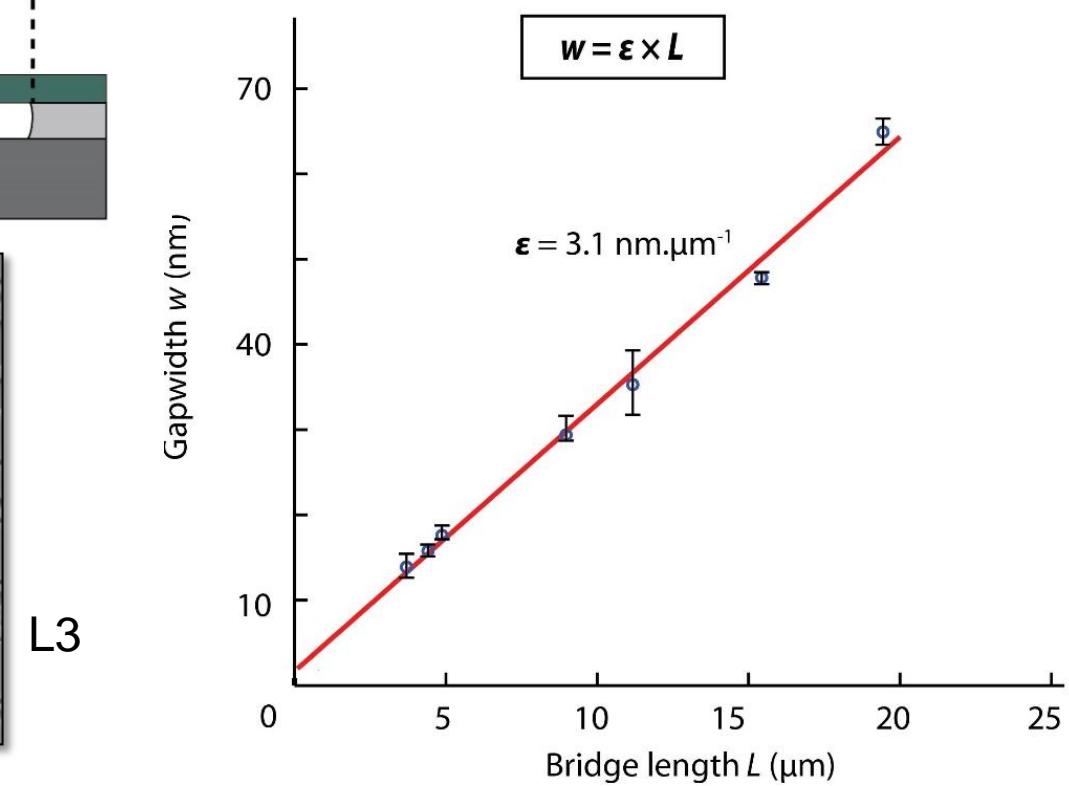
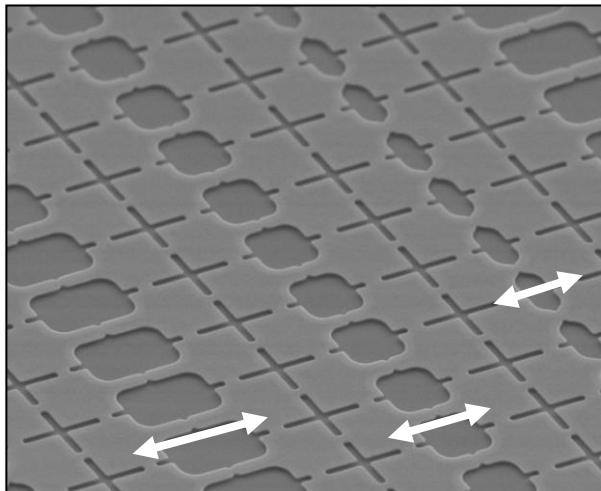
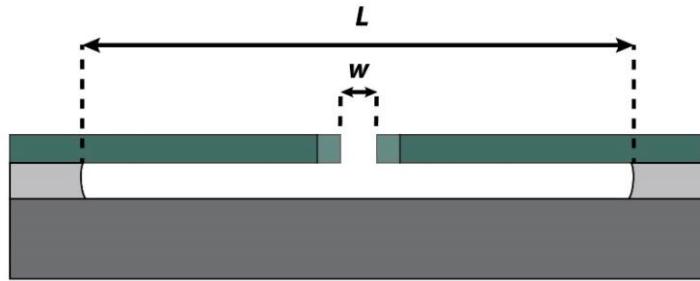
Scalable Fabrication of Crack-Defined Nanogap Electrodes



- Control of gap size: 1-100 nm
- Realization of tunneling junctions
- Massively parallel fabrication

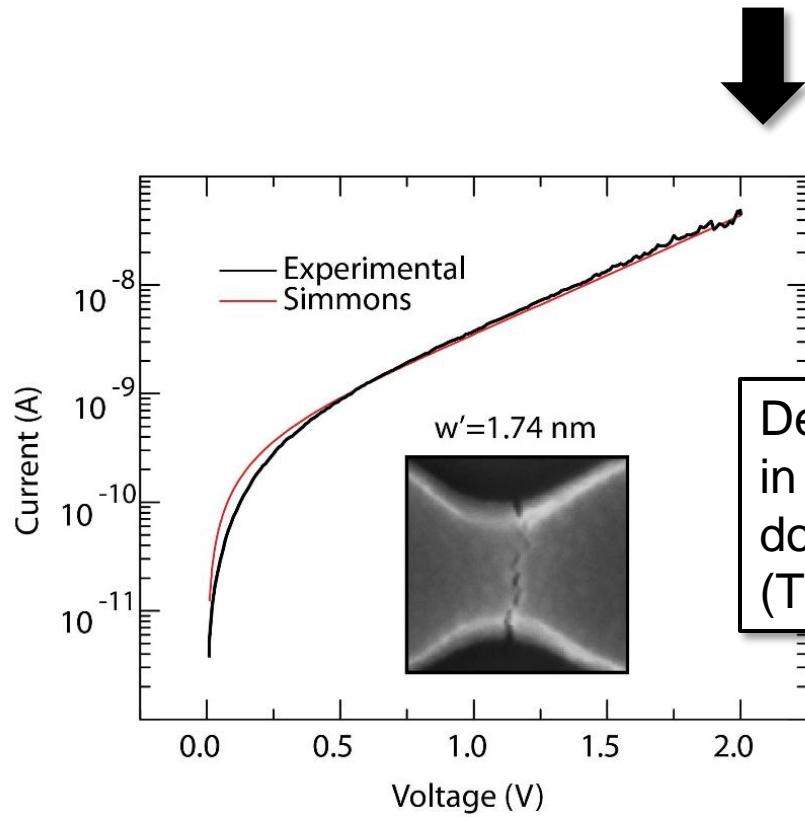
Control of Gap Size

1 μm in electrode bridge length \longleftrightarrow 3.1 nm in nanogap width



Nanogap Tunneling Junctions

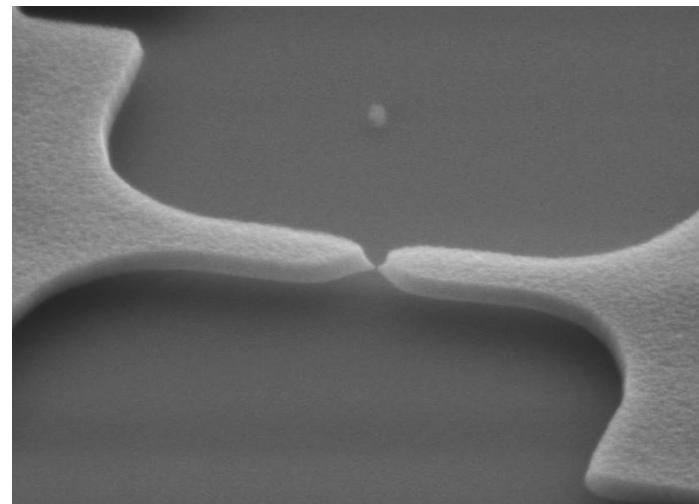
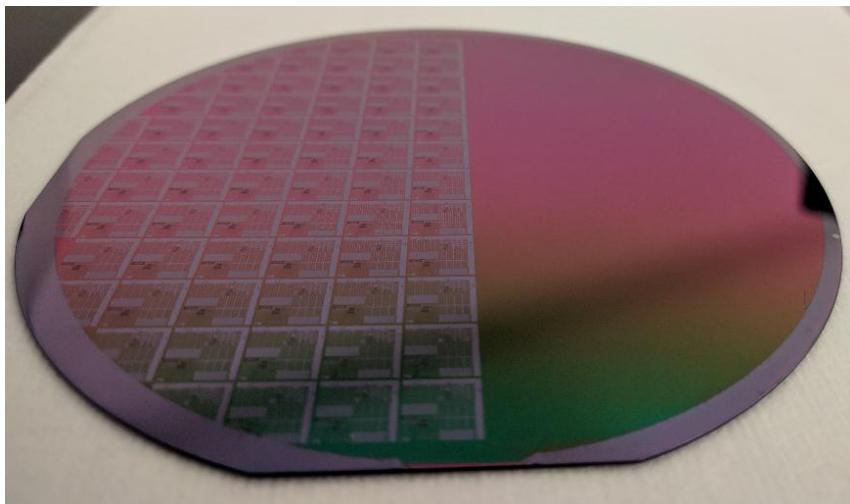
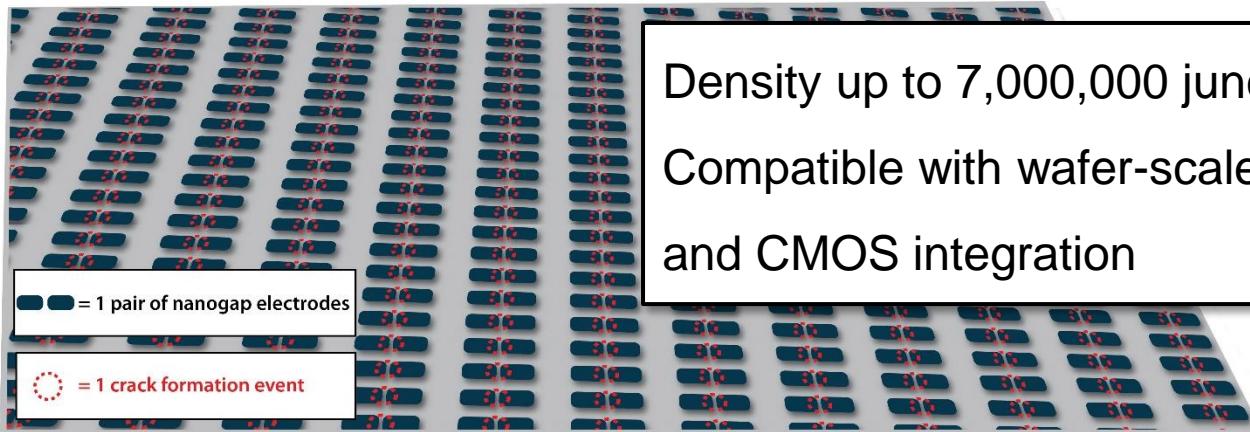
Electron quantum tunneling occurs with **sub-3 nm nanogaps**



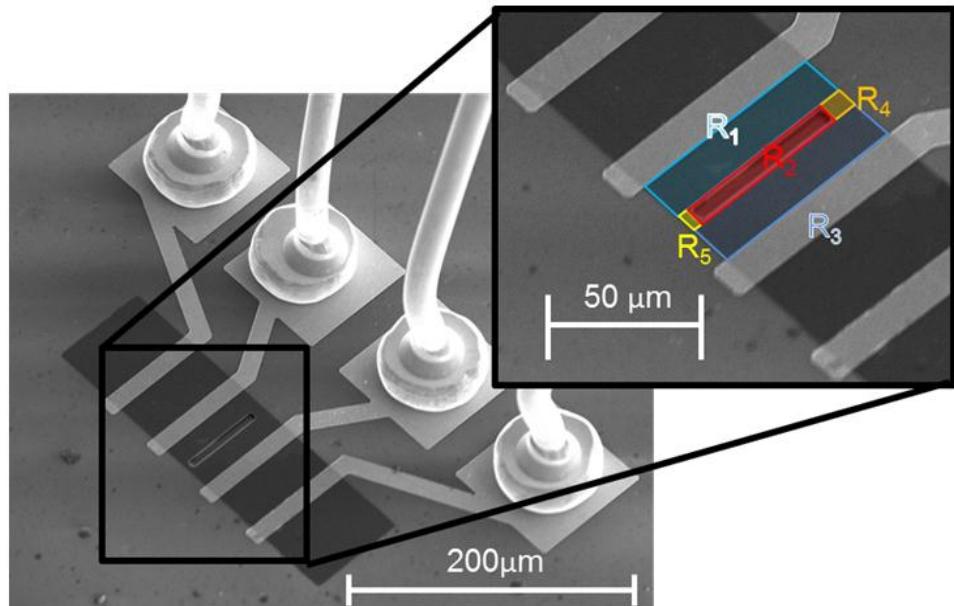
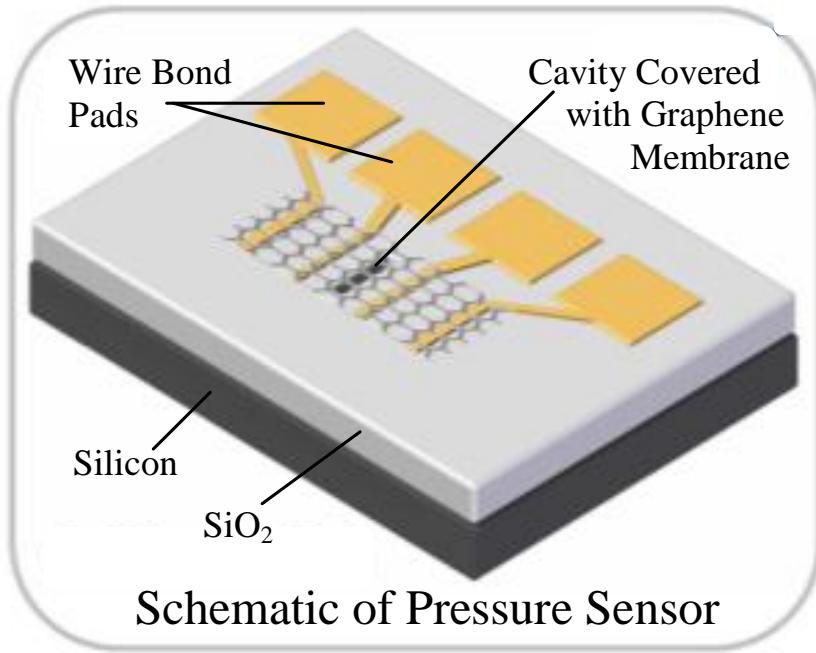
Demonstration of quantum tunneling in crack-defined nanogap electrodes down to **sub-1 nm** in titanium nitride (TiN) and gold (Au)



Massively Parallel Fabrication

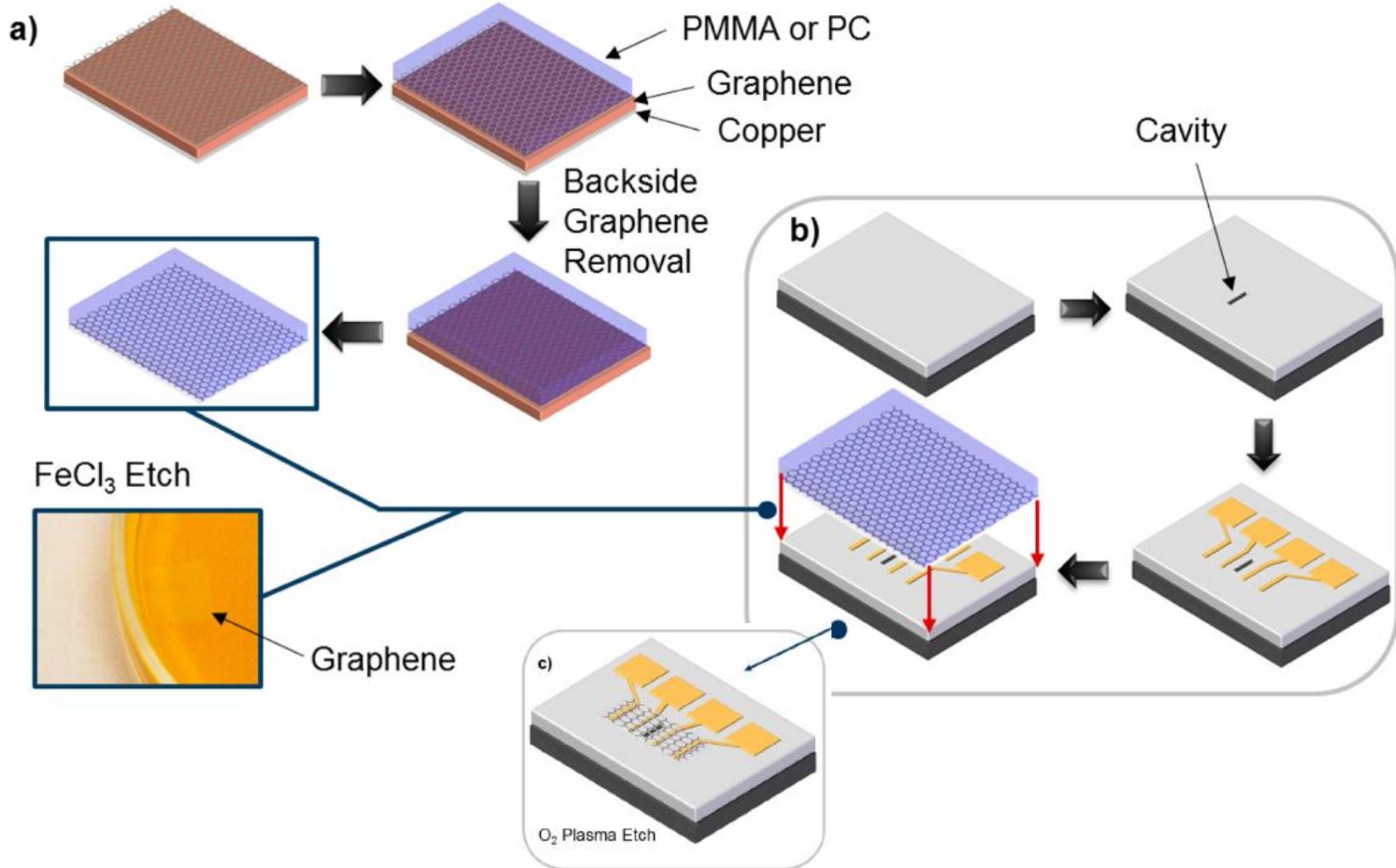


Graphene-Based NEMS: Pressure Sensing



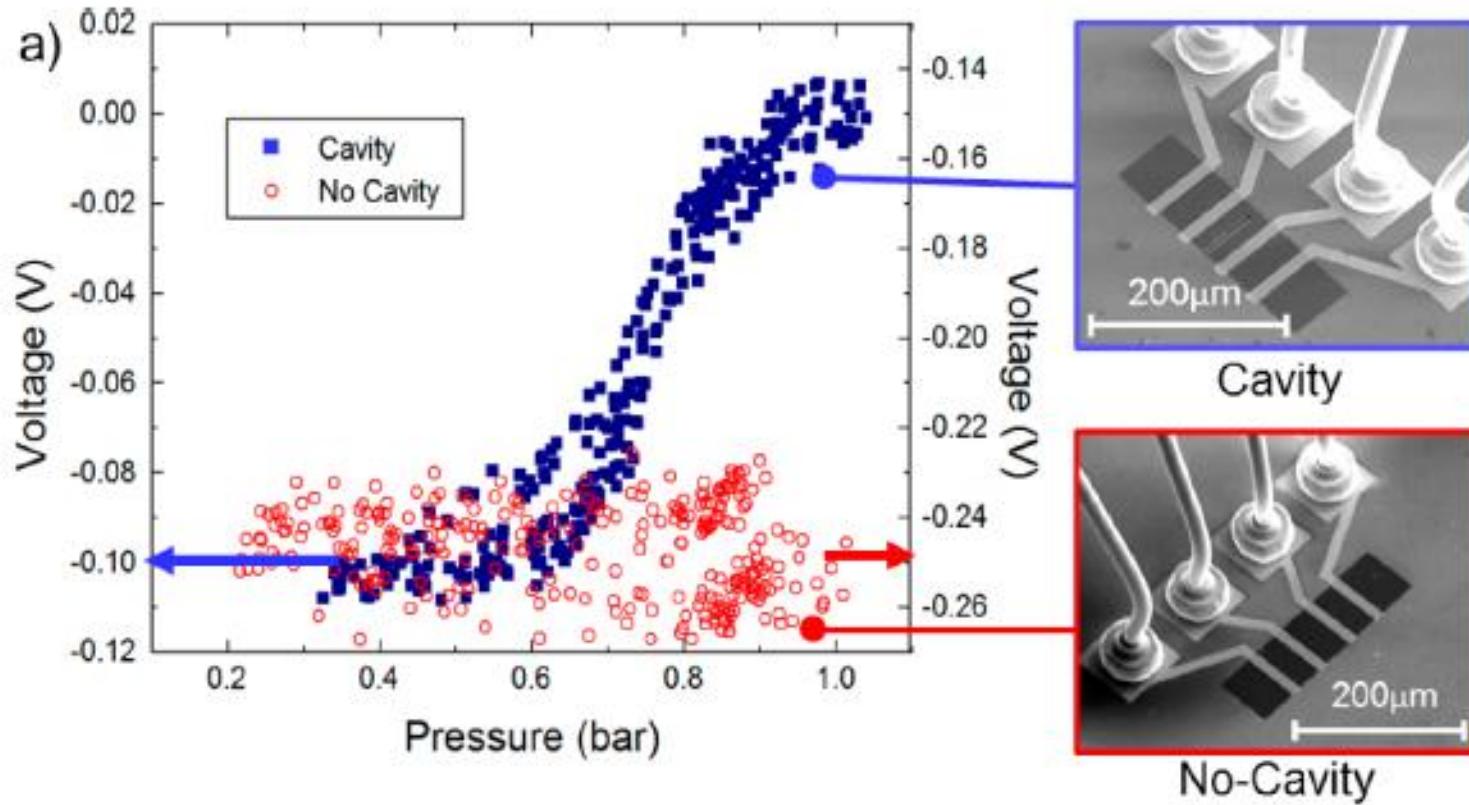
Smith, A. D., Niklaus, F., Paussa, A., Vaziri, S., Fischer, A. C., Sterner, M., ... & Ostling, M. (2013). Electromechanical piezoresistive sensing in suspended graphene membranes. *Nano letters*, 13(7), 3237-3242.

Graphene-Integration in NEMS



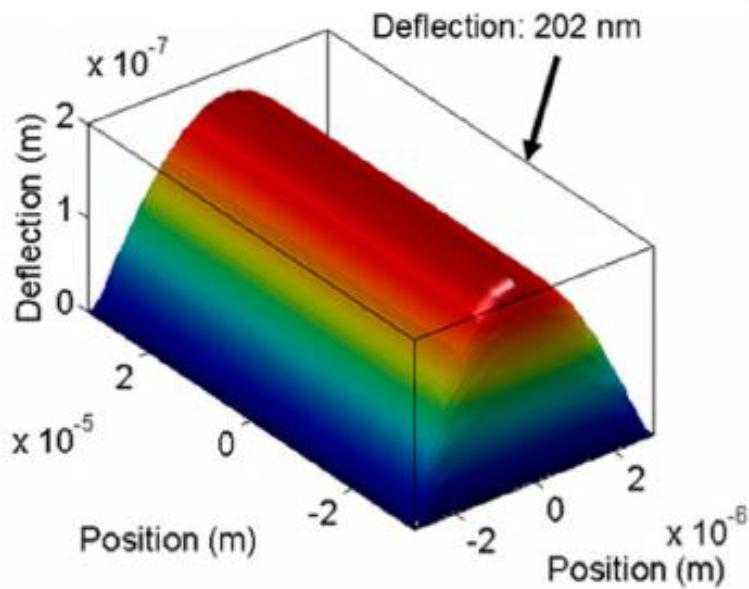
Smith, A. D., Niklaus, F., Paussa, A., Vaziri, S., Fischer, A. C., Sterner, M., ... & Ostling, M. (2013). Electromechanical piezoresistive sensing in suspended graphene membranes. *Nano letters*, 13(7), 3237-3242.

Graphene-NEMS Pressure Sensing

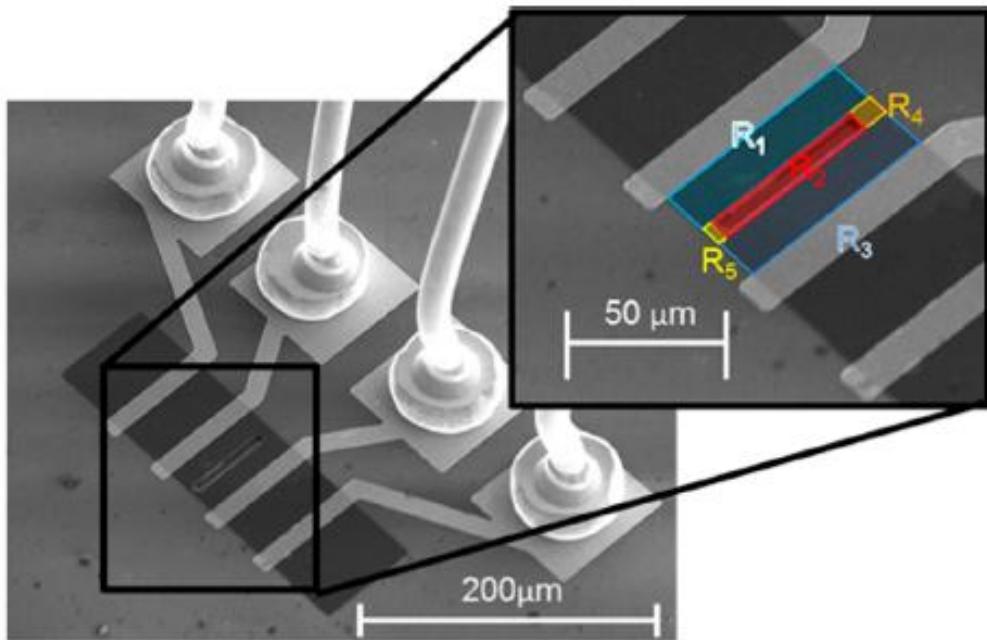


Smith, A. D., Niklaus, F., Paussa, A., Vaziri, S., Fischer, A. C., Sterner, M., ... & Ostling, M. (2013). Electromechanical piezoresistive sensing in suspended graphene membranes. *Nano letters*, 13(7), 3237-3242.

Graphene-NEMS Pressure Sensing



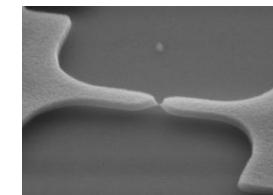
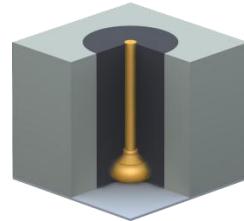
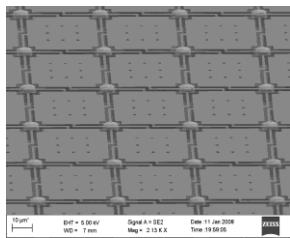
b)



Smith, A. D., Niklaus, F., Paussa, A., Vaziri, S., Fischer, A. C., Sterner, M., ... & Ostling, M. (2013). Electromechanical piezoresistive sensing in suspended graphene membranes. *Nano letters*, 13(7), 3237-3242.

Summary

- Heterogeneous 3D integration platform for micro-mirrors, IR bolometers and NEMS relays.
- Wafer-level vacuum packaging, and wire bonding and magnetic assembly for wire integration in MEMS.
- Graphene NEMS pressure sensors and nanofabrication technologies for tunnelling junctions.





Acknowledgements

Funding Sources



*Knut och Alice
Wallenbergs
Stiftelse*



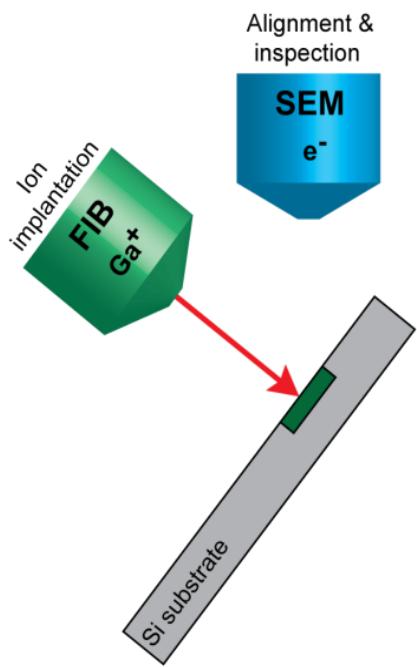
Collaboration Partners



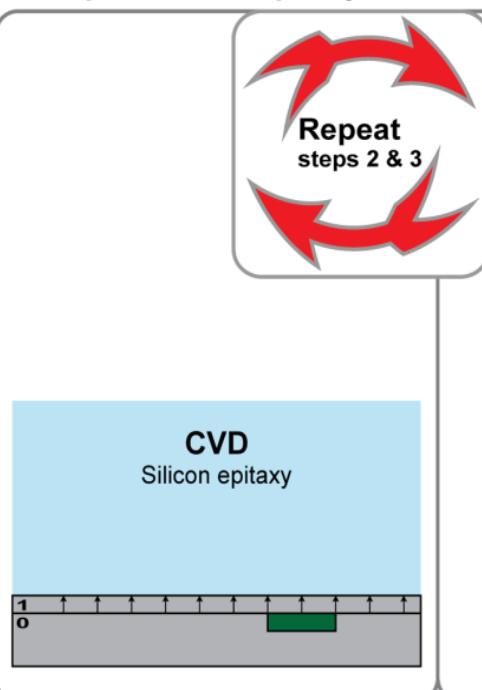


3D Printing Process for Si Nano Devices

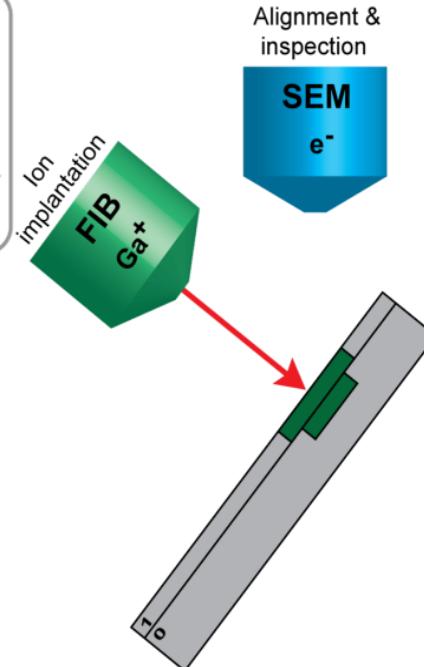
Step 1: Implantation



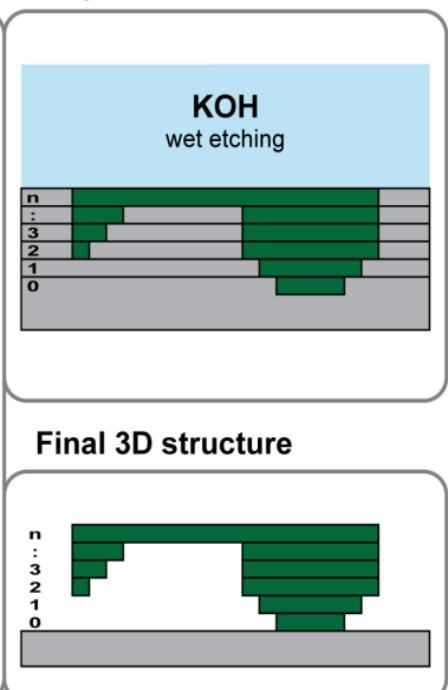
Step 2: Silicon Epitaxy



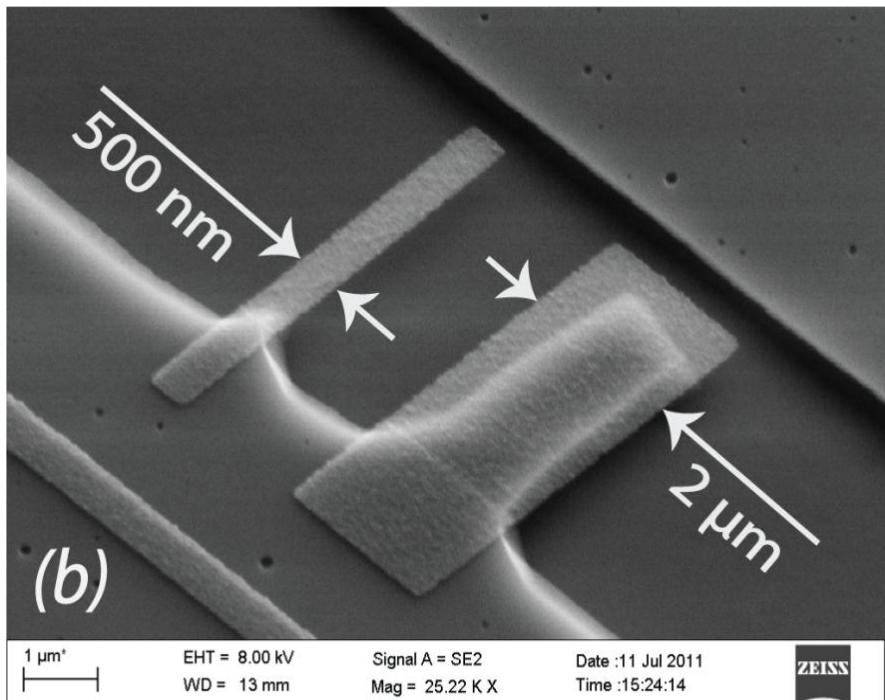
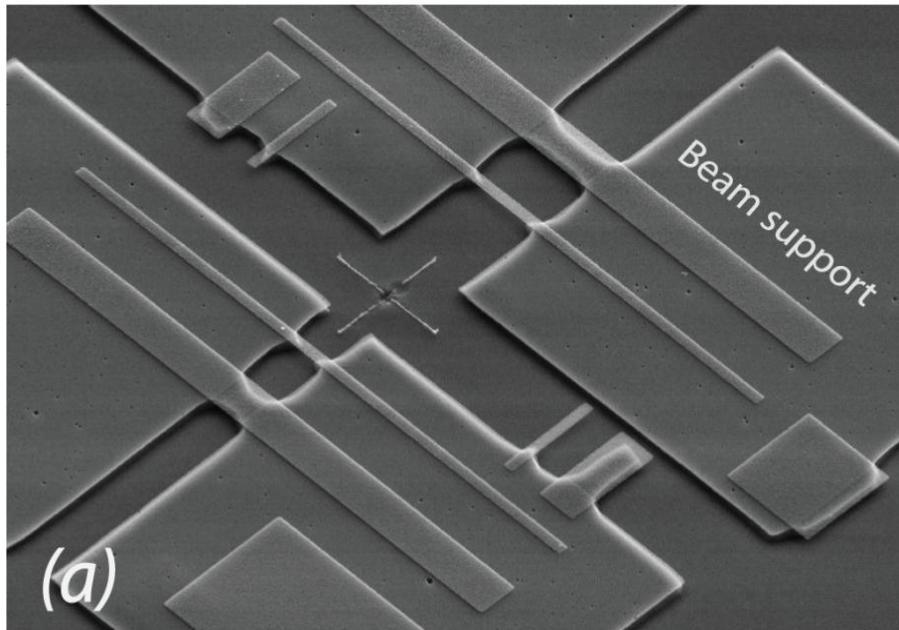
Step 3: Implantation



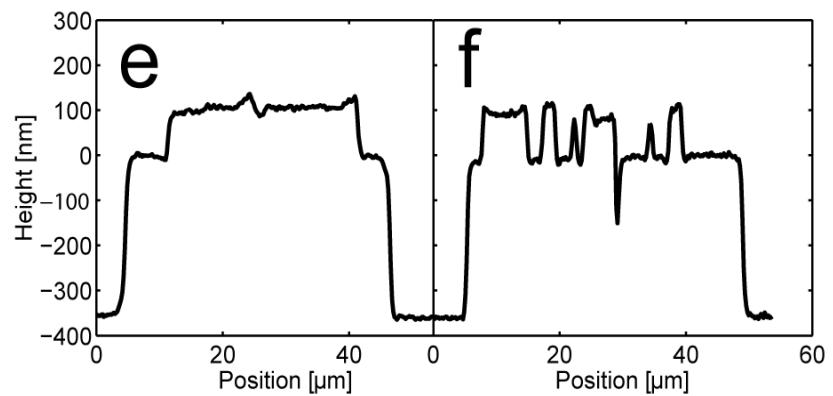
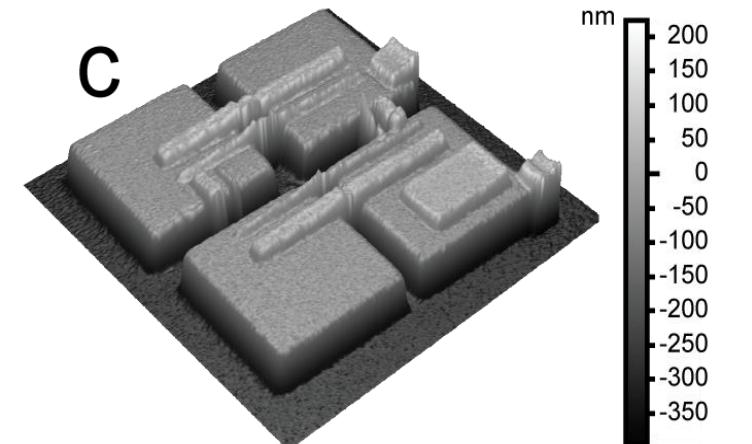
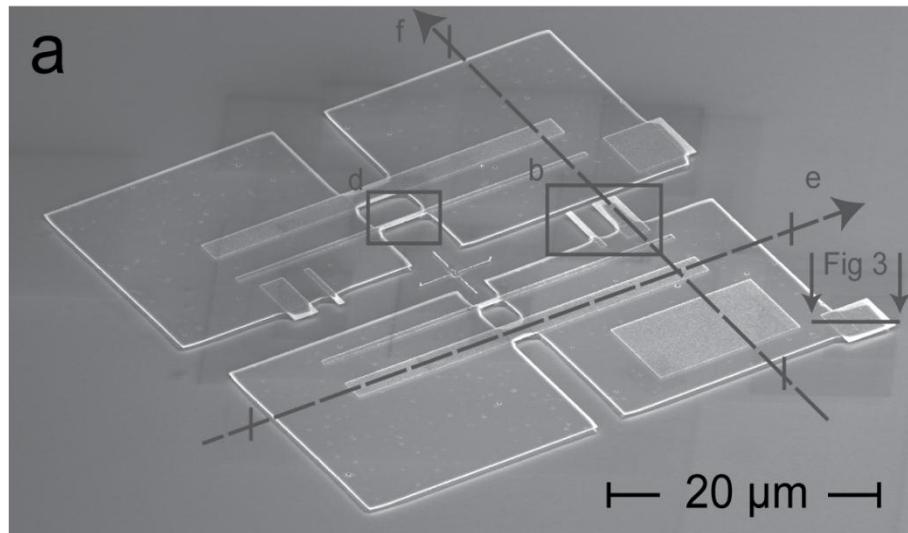
Step 4: Free etch



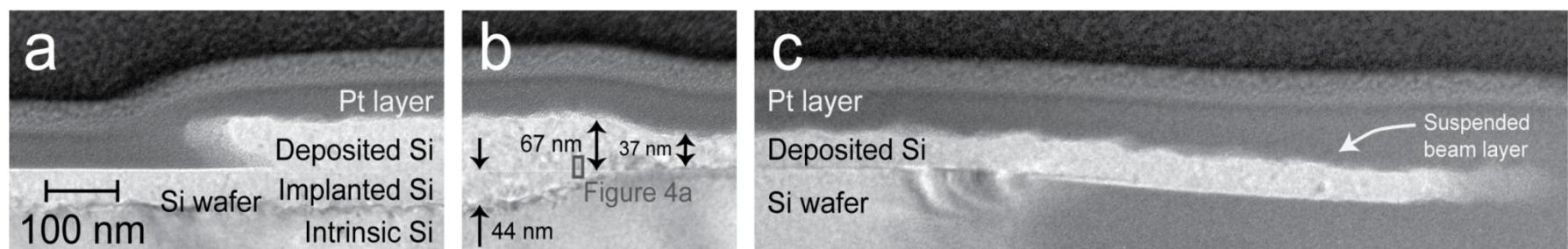
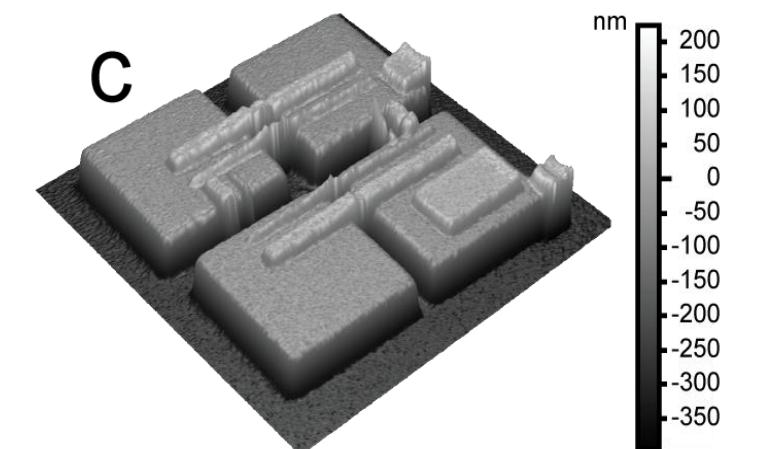
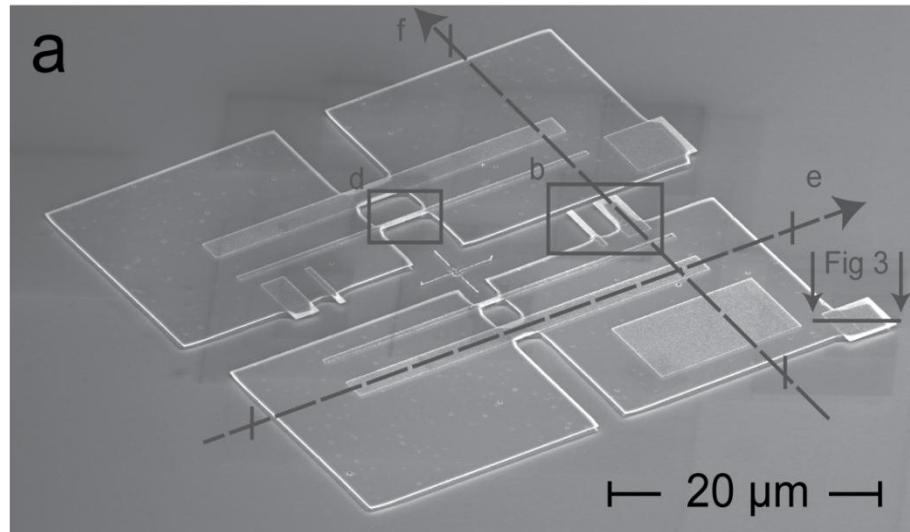
3D Printing of Si Micro and Nano Devices



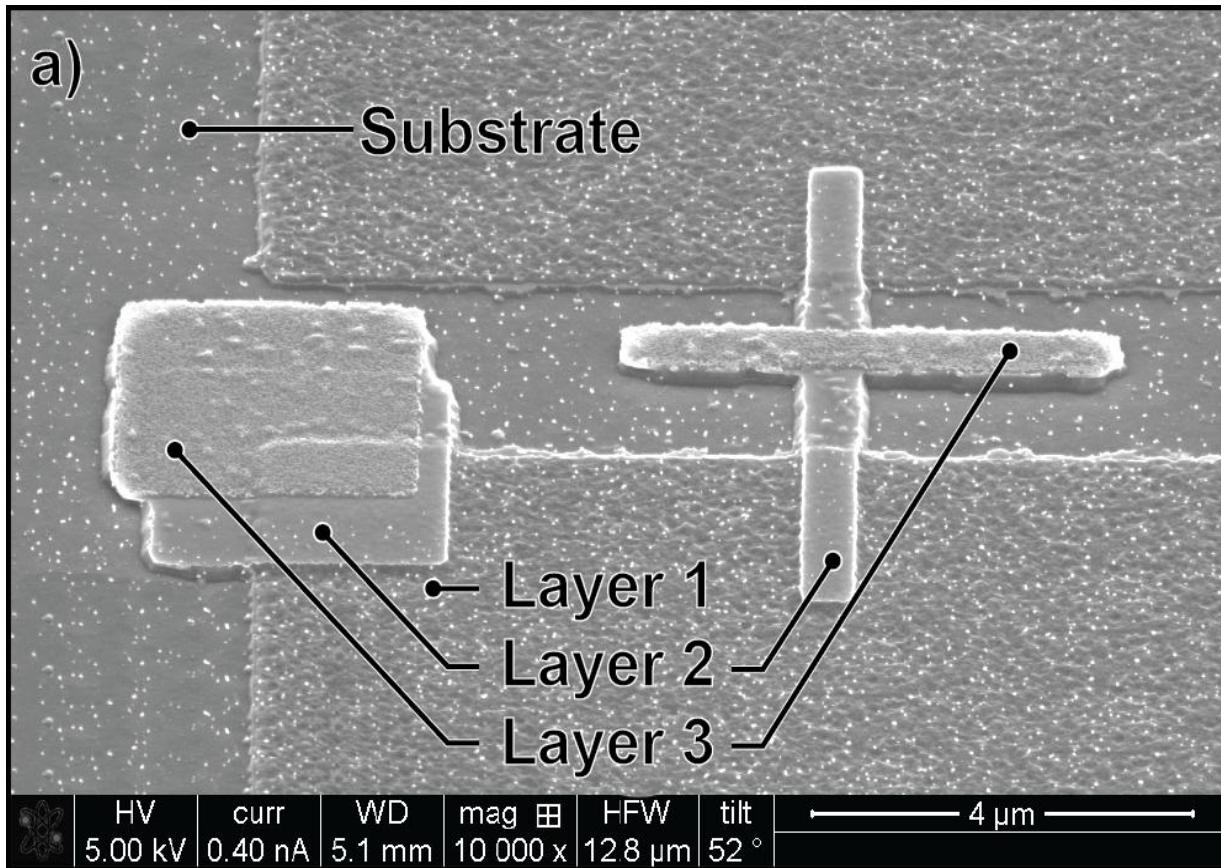
3D Printing of Si Micro and Nano Devices



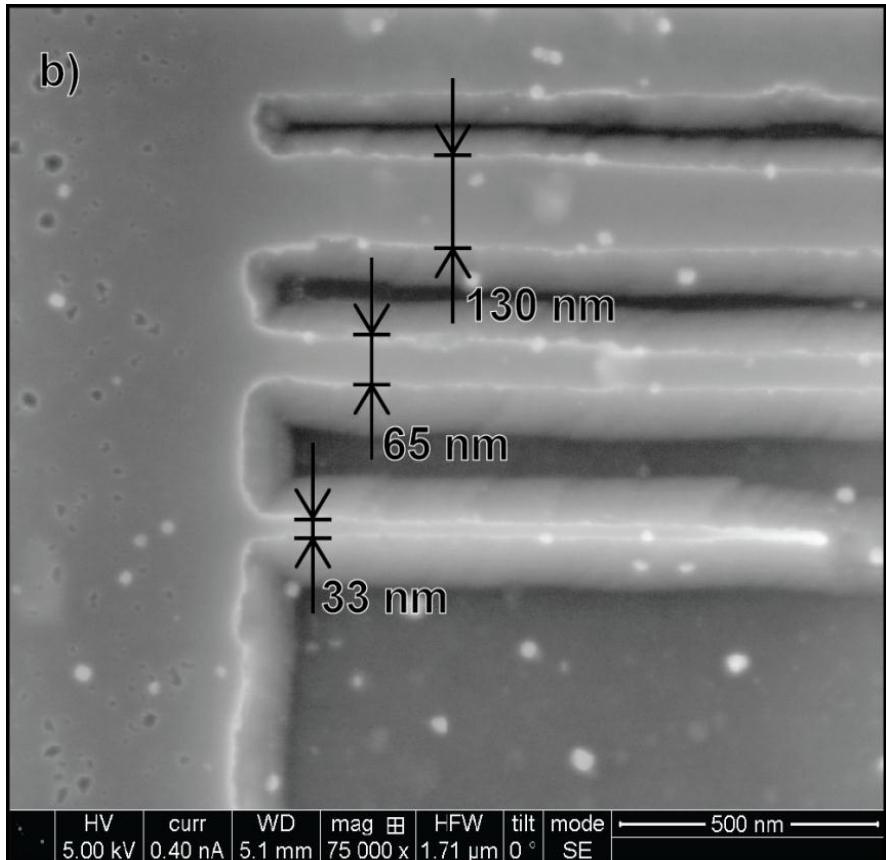
Cross Section of Si Nano Devices



3-Layer 3D Printed Si Micro-Structures



Resolution Limits of 3D Si Printed Nano-Structures



- Line-width resolution of 33 nm demonstrated.
- Line-width resolution of 20 nm with FIB writing, reported in literature.
- Layer thickness on the order of 35-70 nm.