INTEGRATION OF DIAMOND MICROELECTRODES ON CMOS-BASED AMPEROMETRIC BIOSENSOR ARRAY BY FILM TRANSFER TECHNOLOGY

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This paper is the first report on the integration of boron-doped diamond (BDD) microelectrodes with excellent electrochemical properties on CMOS-based 20×20 amperometric biosensor array (Fig. 2). The fully-integrated device detected histamine and dopamine owing to a wide potential window of the BDD electrode (Fig. 4), and offered 2-dimensional real-time imaging of dopamine diffusion in a solution (Fig. 5). The BDD electrodes were once formed on a Si wafer at 800°C, and then transferred to a 0.18 μm CMOS wafer with a benzocyclobutene (BCB) bonding interlayer (Fig. 1).

CMOS-based amperometric sensor arrays with metal electrodes such as Au or Pt ones have been developed for the electrochemical imaging of various biomolecules [1, 2]. However, detectable analytes are limited due to a narrow potential window and large background current of the metal electrodes. One of the best electrochemical electrode materials is BDD, which has a wider potential window and smaller background current. BDD is normally prepared by chemical vapor deposition (CVD) at high temperature such as 800°C, and thus not compatible with CMOS circuits. Therefore, we propose to employ film transfer technology for the monolithic integration of BDD microelectrodes on a CMOS-based amperometric sensor array.

Figure 1 illustrates the integration process developed in this study. (1) Cr/Pt/Au/Pt/Cr electrodes were patterned on a 0.18 μm CMOS LSI wafer, and (2) BCB was spin-deposited as a bonding interlayer. (3) BDD electrodes on a Si wafer were bonded with the LSI wafer at 270°C. The BDD were synthesized on the Si substrate by plasma-enhanced CVD under the condition shown in Table 1, and patterned in advance. (4) The Si substrate was removed by dry etching. (5) Contact holes were opened on the BCB layer by dry etching, and (6) the BDD electrodes were electrically connected to the LSI with a metal film. (7) Finally, SU-8 microwells were fabricated to define the BDD sensing area.

The integration was completed without any damage in the CMOS circuit owing to low process temperature below 270°C. 20×20 BDD microelectrodes are arrayed with a pitch of 250 μm, and each electrode provides an active area of 40 μm diameter, as shown in Fig. 2(a) and (b). The transferred BDD electrodes were highly dense polycrystalline without voids and cracks (Fig. 2(c)). The diced chip was mounted on an Au-metallized ceramic substrate and wire-bonded. Then, a polydimethylsiloxane pool was formed on the ceramic substrate to keep a sample solution, as shown in Fig. 2(d).

A measurement setup is illustrated in Fig. 3. Reference and counter electrodes were dipped in an electrolyte. Figure 4(a) clearly exhibits that the integrated BDD electrodes have a wider potential window and smaller background current compared to an Au electrode. The cyclic voltammogram of ferrocenemethanol (Fig. 4(b)) presents an ideal redox current profile specific to microelectrodes owing to smooth electron transfer. As shown in Fig. 4(c), the sensor amperometrically detected histamine with high oxidation potential around 1.3 V, which is too high for a conventional Au electrode to detect because of a large oxidation current of hydroxide ions in water generated at lower potential. The oxidation current of dopamine, which is one of important biomolecules, was also detected around 1.1 V (Fig. 4(d)), and its diffusion behavior in a solution was imaged in real time by parallel measurement of redox current at 400 points (Fig. 5).

In conclusion, this study developed the film transfer integration process of BDD microelectrodes on the CMOS-based amperometric sensor array and demonstrated its excellent sensing performance compared with metal electrode sensors. This type of integrated biosensor promises sensing and imaging applications of various important biological materials, which cannot be detected by conventional sensors.

References
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1. Cr/Pt/Au/Pt/Cr patterning

2. BCB coating and alignment of BDD electrode with the metal pattern.

3. Bonding of LSI and Si substrate.

4. Remove Si substrate by dry etching.

5. BCB patterning by dry etching.

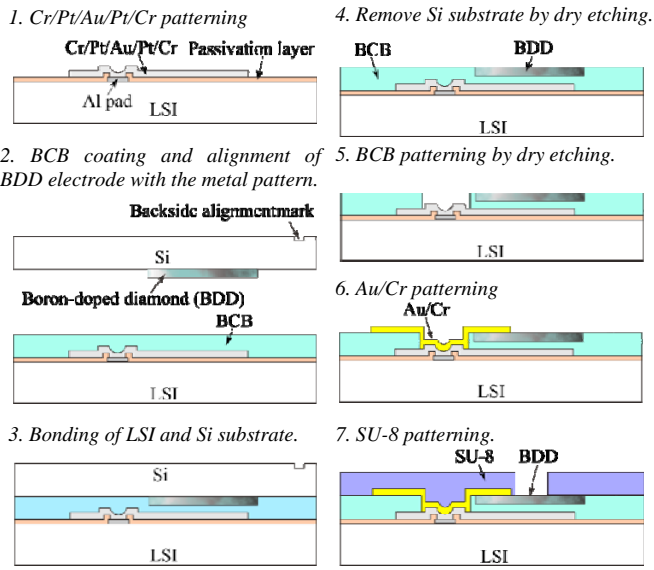6. Au/Cr patterning

7. SU-8 patterning.

Figure 1: Fabrication process of CMOS-based amperometric biosensor array with Boron-doped diamond (BDD).

Table 1: Condition of BDD synthesis by plasma-enhanced CVD.

Power	Pressure	H$_2$ flow	CH$_4$ flow	B(OCH$_3$)$_3$ flow	Growth temperature
1 kW	6.5 kPa	300 sccm	3 sccm	0.18 sccm	800 ℃
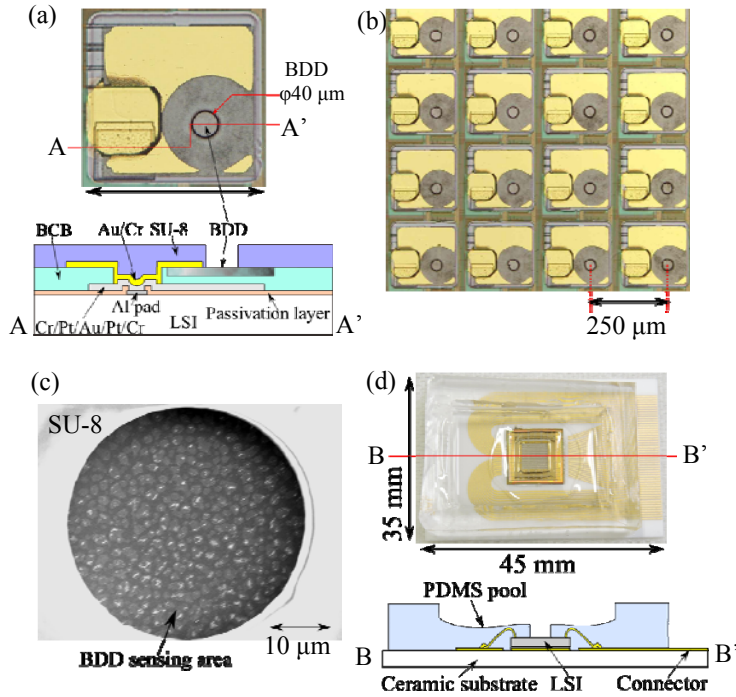
Figure 2: (a) Optical microscope image and schematic cross sectional view along A-A' line of the single unit cell in the integrated amperometric sensor. (b) Unit cell array (c) Scanning electron micrograph of the BDD electrode surface (d) Completed device mounted on the ceramic substrate with a polydimethylsiloxane (PDMS) pool for electrochemical measurement experiments. Lower image is the schematic cross sectional view along B-B' line.
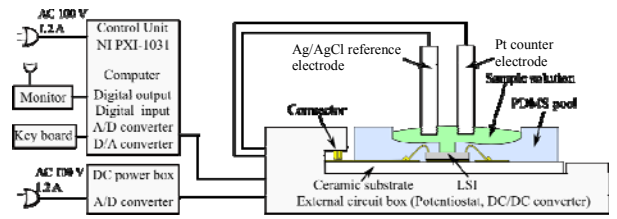

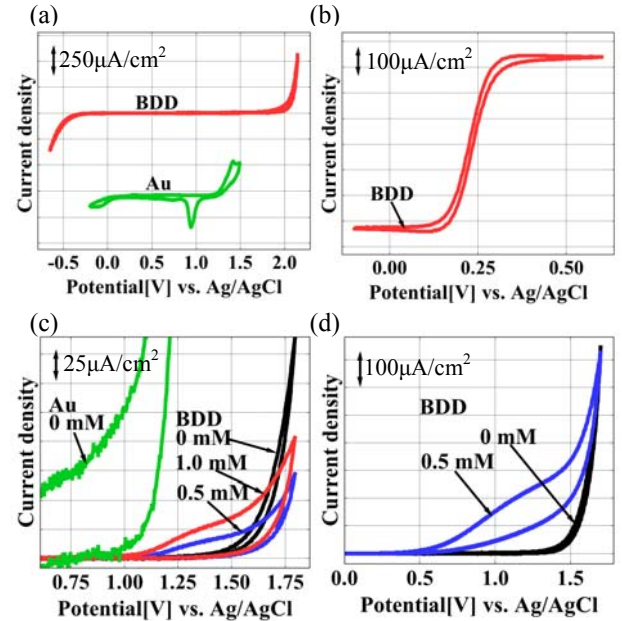Figure 3: Schematic of measurement system for the BDD electrode integrated amperometric sensor.

Figure 4: Typical cyclic voltammogram of (a) 0.5 M H$_2$SO$_4$, (b) 2 mM ferrocenemethanol in 0.1 M KCl, (c) 0–1.0 mM histamine in Dulbecco's phosphate buffer saline (PBS) (d) 0 and 0.5 mM dopamine in the PBS. These scan rates, 20 mVs^{-1}.
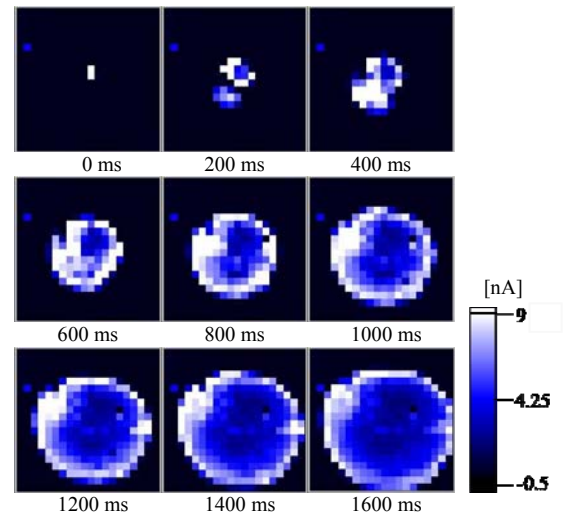

Figure 5: 2D imaging of dopamine diffusion dissolved in the PBS near the center position of the BDD electrode array. Color maps correspond to the redox current intensities of 400 electrodes at 1.2 V.

A 1.7MM^3 MEMS-ON-CMOS TACTILE SENSOR USING HUMAN-INSPIRED AUTONOMOUS COMMON BUS COMMUNICATION

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A bus-connected tactile sensor system composed of MEMS-CMOS integrated force sensors was developed. A capacitor-to-digital convertor for force sensing, a data reduction processor and a serial bus communication controller are implemented by a laboratory-designed integrated ASIC. These functions enable the tactile sensor to be connected serially, and to autonomously transmit the sensing data using CSMA (Carrier Sense Multiple Access) protocol (Fig. 1). A novel MEMS-CMOS integration technology[1] was applied, so that the integrated tactile sensor can be directly mounted on a flexible printed circuit board. The chip size is 2.54mm × 2.54mm × 0.27mm, i.e. 1.7mm^3, and there are 16 through silicon interconnection using the lateral tapered groove (Fig. 2). The digital data from the completed tactile sensor contains 32-bits force sensing data, which corresponds to an external force linearly with 8bit/N resolution at 6.25Hz sampling (Fig. 3). Since the drastic decrease of data collision rate was expected, human-inspired threshold-based operation and adaptation were carried out to reduce the non-critical tactile data (Fig. 4). Finally, the serial bus network was demonstrated to estimate the network performance (Fig. 5)

Figure 1 shows the overview of the tactile sensor system. The flexible cable is a common bus line composed of 2 power lines (V18, V33), 1 signal line (DATA) and 1 ground line (GND). Reducing wires and data quantity are critical problems to achieve the whole body tactile sensation for robot[2]. To address the problems, we adopted a human-inspired autonomous common bus communication. Figure 2 shows the fabricated integrated device. The surface mountable tactile sensor were prototyped by a fabrication process using "through silicon groove" interconnection technology and wafer bonding.

Figure 3 shows the measured output signals from the completed integrated device. The data field includes converted force data. Since force-to-capacitance conversion by the MEMS and capacitance-to-frequency conversion by the circuit canceled their parabolic characteristic of transduction each other, the linear response of the digital output with external force was obtained. This result well agrees with mechanical and electrical simulations. The deformation of the diaphragm was 300nm and capacitance change was 10fF, when applying 1N normal force.

The demonstration of data reduction was examined using a chip as shown in Fig. 4. After the tactile sensor was initialized, data was transmitted continuously at a frequency of 5.5kHz (Fig. 4 (a)). By the threshold operation, the number of the tactile data was reduced by 59% (Fig. 4 (b)). In the threshold-based operation, weak force data below the pre-defined threshold was filtered and not transmitted on the bus. A further data reduction of 37.4% (i.e. 96.7% in total) was achieved in conjunction with adaptation (Fig. 4 (c)). By the adaptation, transmission interval time was lineally increasing during applying constant strong forces over the threshold value.

Although autonomous bus communication using CSMA protocol improves response time to external forces compared with the polling protocol, the packet collision will become a critical problem as the packet quantity increases. Therefore, the collision rate was experimentally measured in a small system composed of the three sensor nodes. Figure 5 shows the collision rate and throughput as a function of the packet generation rate, which are calculated from the acquired bus signals. In this experiment, every sensor node transmits the signals without the data reduction. The highest data throughput (73%, 1Mbps) was obtained when all of the sensors transmit each data at 4.6kHz. We obtained the fact that the collision rate is negligible when the throughput is less than about 50%. Since 90% reduction of tactile data can be achieved by the adaption like Fig.4, both of low-collision and fast response data transmission can be realized in this system.
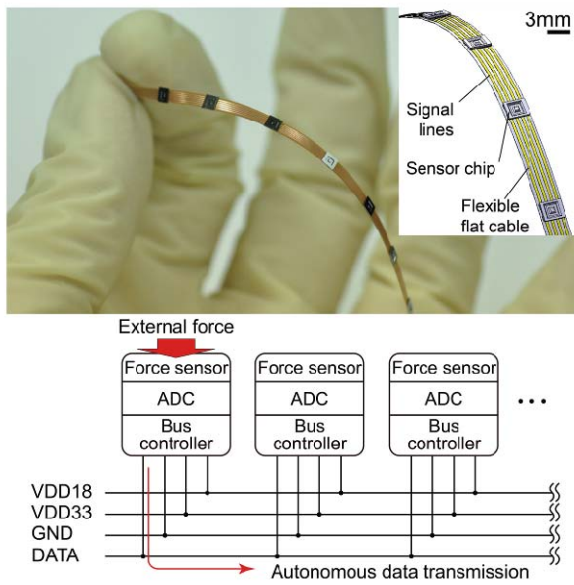
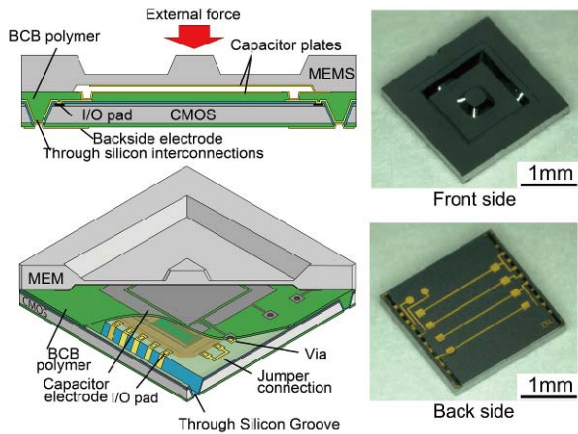*Figure 1: Tactile sensor using autonomous common bus communication.*

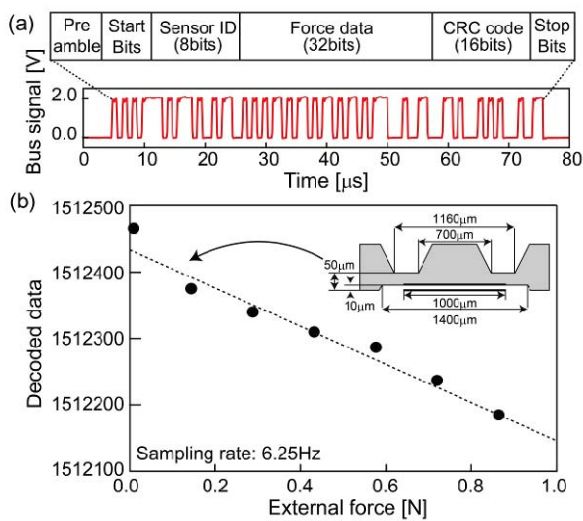*Figure 2: Device structure and completed tactile sensor chip.*

Figure 3: Output signal and its properties of the integrated tactile sensor (a)Digital output (b)Response to external force.
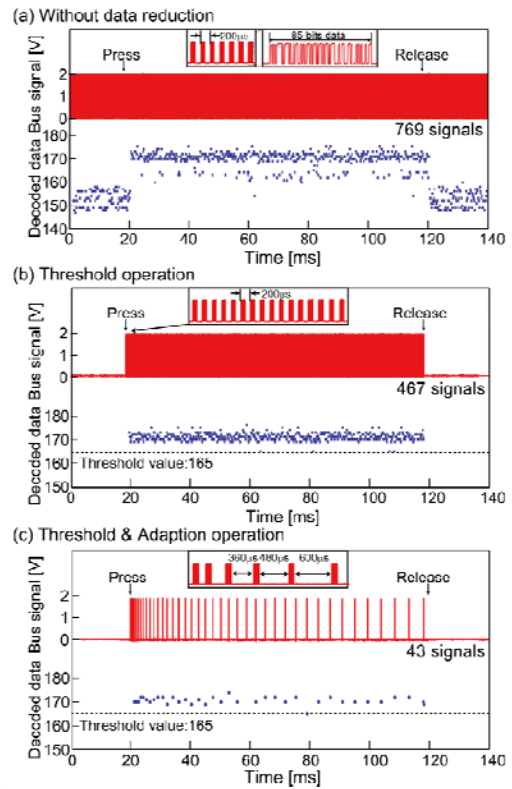

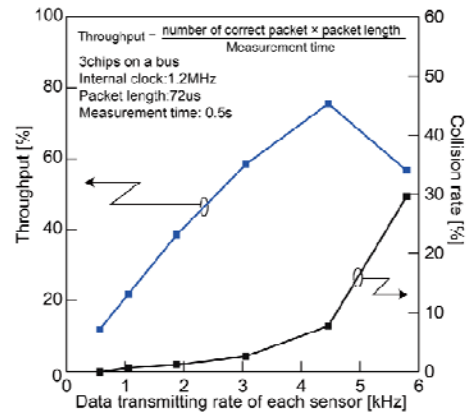*Figure 4: Data transmission with/without data reduction.*

Figure 5: Data collision rate as a function of sampling rate of a single chip.

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Low-Voltage PZT-Actuated MEMS Switch Monolithically Integrated with CMOS Circuit

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MEMS switches actuated by PZT at low voltage were integrated with 0.35μm CMOS **(Fig. 1 and 4)**. To our best knowledge, this is the first PZT-actuated switch really fabricated on a CMOS wafer (not a dummy wafer). A preliminary test confirmed that the switch and the CMOS circuit **(Fig. 2)** worked **(Fig. 5 and 6)**. PZT must be deposited at high temperature, and thus not CMOS-compatible. To overcome this limitation, we fabricated switch structures on a Si dummy wafer using PZT sol-gel method, and then transferred them to the CMOS wafer by polymer bonding. After the dummy wafer was removed, the switch structure and the CMOS circuit were connected by Au electroplating. Finally, the polymer was sacrificially etched by O_2 plasma to release the switches. This integration process can be applied to other functional materials difficult to deposit on CMOS wafers.

The monolithic integration of MEMS switches with CMOS will add new functionality to integrated circuits, e.g. frequency tunability and area-by-area breaker function. CMOS-integrated MEMS switches were already reported [1], but none of them used PZT actuation. Electrostatic actuation generally needs high driving voltage, which is difficult to directly supply from a standard CMOS circuit. Narrowing the capacitance gap to ~1μm considerably lowers driving voltage [2], but RF isolation and yield are also lowered. Another problem is their relatively large size. For higher actuation force, electrostatic actuators should be larger, but this limits the number of the devices which can be mounted on a limited die area. On the other hand, PZT actuators can be driven at a few V, if the PZT layer is thin (e.g. <500nm). In addition, they does not show pull-in phenomenon, and thus continuous change of the gap to zero is possible, which is advantageous for variable capacitor applications.

However, PZT is not a CMOS-compatible material, because the deposition needs high temperature of 600~700°C. To overcome this problem, wafer-level transfer technology reported in [3,4] can be used. The basic idea is that PZT-based MEMS fabricated on a dummy wafer is transferred to a CMOS wafer. The previous papers said that the process was "CMOS-compatible", but actually the devices were fabricated on a Si or glass wafer. In this study, we fabricated PZT-actuated switches shown in **Fig. 1** on 0.35μm CMOS. **Figure 2** shows the fabrication process. On a Si wafer with TiO_2 diffusion barrier, two stacks of Ti/Pt/PZT/Ti/Pt layer are formed. The PZT is 750nm thick and deposited by sol-gel method at 680°C. The switch structure is defined by RIE and Au contacts are formed. The CMOS wafer is planarized by SiO_2 deposition and polishing, and then Au electrodes are fabricated on it. Both wafers are covered by aromatic polymer (7μm thick in total), and bonded at 150°C with 1MPa pressure. After etching way the dummy wafer, via holes are fabricated by RIE. Electrical connection is established by filling the via holes with electroplated Au. Finally, the polymer is ashed away to release the switch.

Figure 3 shows the fabricated device. The CMOS circuit is a simple 4-bit switching circuit using D flip-flop shown in **Fig. 4**. The fabricated device was preliminarily tested. **Figure 5** shows the output from the CMOS circuit, demonstrating the switching function worked well. **Figure 6** shows the relationship between driving voltage and the displacement of the cantilever. The displacement was measured at the end of the cantilever. At V_{dd}=3.3V, the contact moves ca. 2μm, which is unfortunately smaller than the initial gap due to cantilever bending. In conclusion, we integrated the low-voltage PZT-actuated MEMS switches really on the CMOS wafer, and confirmed the basic operation.

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[4] Farizah Saharil *et al.*, "Low-Temperature CMOS-Comatible 3D-Integration of Monocrystalline-Silicon Based PZT RF MEMS Switch Actuators on RF Substrates", MEMS2010, pp.47–50
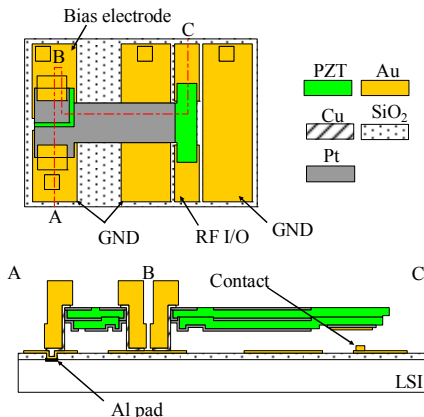
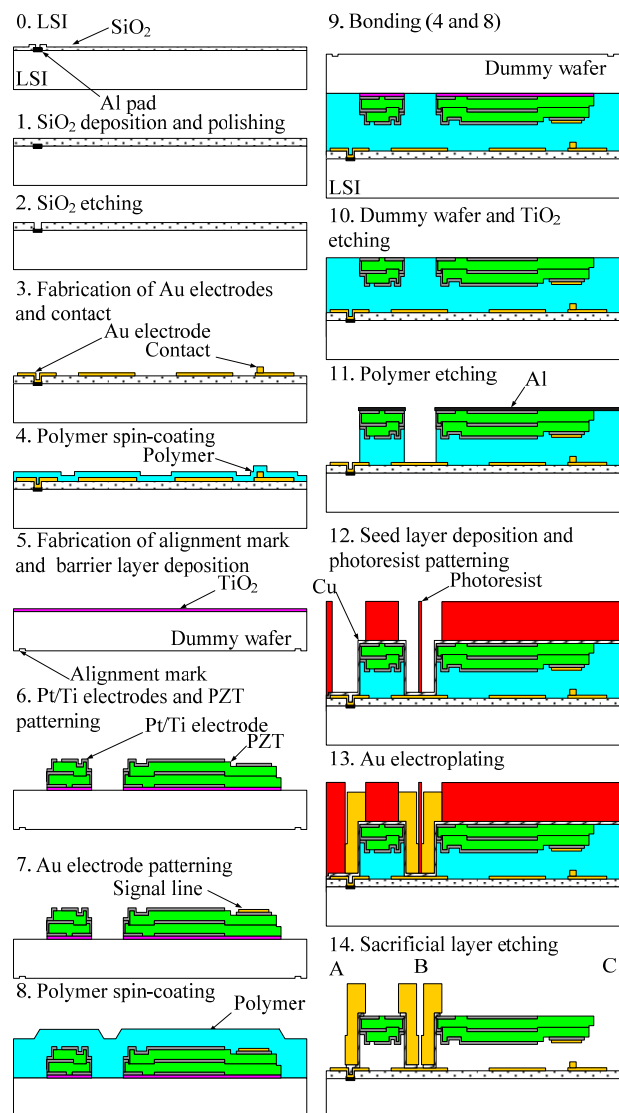**Figure 1** Structure of a PZT MEMS switch integrated with a CMOS circuit

PZT | Au
Cu | SiO₂
Pt

B | C
A
GND | RF I/O | GND

A | B | C
Contact
Al pad
LSI

Figure 1 Structure of a PZT MEMS switch integrated with a CMOS circuit

Figure 2 Process flow

0. LSI
SiO₂
LSI
Al pad

1. SiO₂ deposition and polishing

2. SiO₂ etching

3. Fabrication of Au electrodes and contact
Au electrode
Contact

4. Polymer spin-coating
Polymer

5. Fabrication of alignment mark and barrier layer deposition
TiO₂
Dummy wafer
Alignment mark

6. Pt/Ti electrodes and PZT patterning
Pt/Ti electrode
PZT

7. Au electrode patterning
Signal line

8. Polymer spin-coating
Polymer

9. Bonding (4 and 8)
Dummy wafer
LSI

10. Dummy wafer and TiO₂ etching

11. Polymer etching
Al

12. Seed layer deposition and photoresist patterning
Cu
Photoresist

13. Au electroplating

14. Sacrificial layer etching
A | B | C

Figure 2 Process flow for the PZT MEMS switch integrated with a CMOS circuit

VDD GND | IN_2 | DOUT_1-4
IN_1 | CLK
G S G
3.0 kV x80.0 375μm
3.0 kV x400 75.0μm
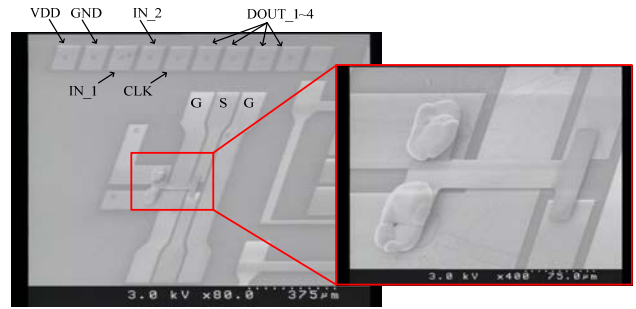
Figure 3 SEM image of the fabricated device

CLK
VDD
Switch Signal
2bit
Delay Circuit
DFF | INV | Out Put "00"
DFF | INV | Out Put "01"
DFF | INV | Out Put "10"
DFF | INV | Out Put "11"
GND
Delay Circuit
INV | INV | INV | INV
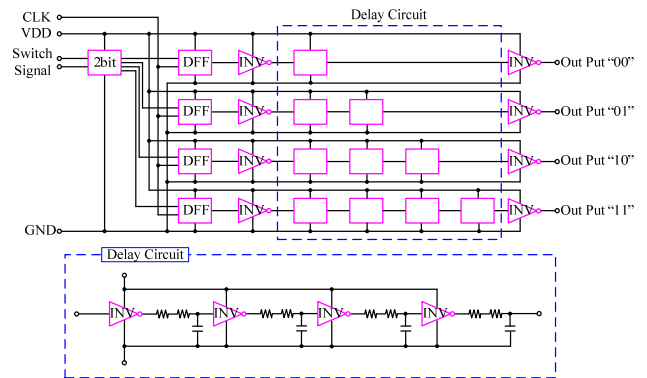
Figure 4 CMOS switching circuit
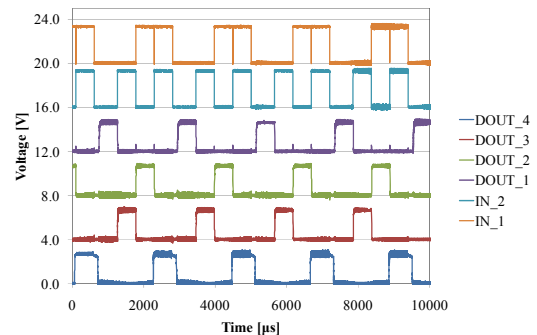
Figure 5 Switching signals from the CMOS circuit under the MEMS switch
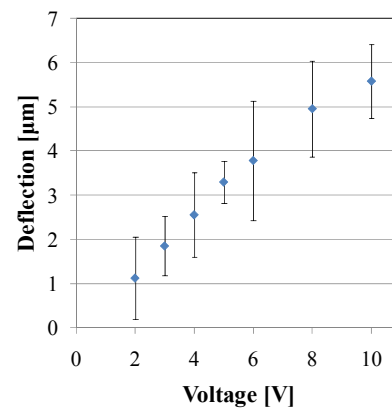
DOUT_4
DOUT_3
DOUT_2
DOUT_1
IN_2
IN_1

Figure 6 Deflection of the MEMS switch cantilever

WIDEBAND TUNABLE LOVE WAVE FILTER
USING ELECTROSTATICALLY-ACTUATED MEMS VARIABLE CAPACITORS
INTEGRATED ON LITHIUM NIOBATE

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[1]Tohoku University, [2]Chiba University

We have demonstrated for the first time a wideband tunable filter in GHz range by directly integrating Love wave (a kind of SAW) resonators with extremely large electromechanical coupling coefficient ($k^2 \sim 30$ %) and electrostatically-actuated MEMS variable capacitors (Figure 4 and 6). A tunable bandpass filters with low insertion loss, sharp cut-off characteristics, wide bandwidth and wide tunability is strongly expected for future reconfigurable and cognitive wireless systems. However, this is very challenging to realize, and no one experimentally demonstrated such a filter to our best knowledge. We confirmed that the 3 dB bandwidth was tuned from 146 MHz to 130 MHz by applying 15 V to the MEMS variable capacitors (Figure 6).

In recent years, the number of wireless services for mobile communication is increasing, and a recent mobile phone can access multiple services at different frequencies. As a result, the wireless front-end, which is composed of filters, amplifiers and mixers, is quite complicated, and thus needs to be simplified for reducing the size and cost. To make a wireless system flexible e.g. for updating the system, a reconfigurable wireless front-end is expected. Furthermore, a cognitive wireless system, which automatically selects the best frequency based on spectrum sensing, is required to solve frequency resource shortage problem. To meet these requirements, a tunable wireless front-end is needed.

The front-end filter must have low insertion loss and sharp cut-off characteristics, and thus acoustic devices such as SAW (surface acoustic wave) and BAW (bulk acoustic wave) devices are used. The resonance frequency of the acoustic devices are basically determined by the dimensions such as IDT (interdigital transducer) pitch and film thickness, which are practically impossible to change widely. Only practical way to change the passband is to connect variable capacitors to the acoustic resonators as shown in Figure 1. However, the tunable range is absolutely limited within the original bandwidth. Therefore, a wideband filter, i.e. a resonator with high electromechanical coupling coefficient (k^2) is necessary to obtain practical tunability. In this study, we have adopted Love wave, which is a kind of SAW with extremely high an electrical mechanical coupling coefficient of $k^2 \sim 30$ %. Love wave is generated on a 15 ° Y LiNbO$_3$ wafer with heavy (e.g. Cu and Au) IDT electrodes [1].

To avoid parastics caused by wire bonding, electrostatically-actuated MEMS variable capacitors, which are schematically shown in Figure 2 (a), were directly integrated on the 15 ° Y LiNbO$_3$ wafer. The variable capacitor was designed using FEM, as shown in Fig. 2 (b), and fabricated according to a fabrication process shown in Figure 3. First, the Love wave filters and IDT fixed capacitors are fabricated by lift-off process. The IDT must be made by heavy metal with a designed thickness to generate Love wave, and Au is used in this study. Next, a sacrificial photoresist layer is formed, and then a Ni layer is selectively electroplated on a Cu seed layer with a photoresist mold. Finally, the Cu seed layer is wet-etched, and the sacrificial photoresist layer is removed by O$_2$ ashing to release the MEMS variable capacitors. Figure 4 shows the optical micrograph of the completed tunable filter. Figure 5 shows the variable capacitor and the Love wave resonator. We obtained a nice bandpass characteristic with a relative bandwidth of 13 %. As shown in Figure 6, the 3 dB bandwidth was tuned from 146 MHz to 130 MHz by applying 15 V to the MEMS variable capacitors. This result is approximately consistent with our simulation result. To our best knowledge, this is the first demonstration of a tunable SAW filter.

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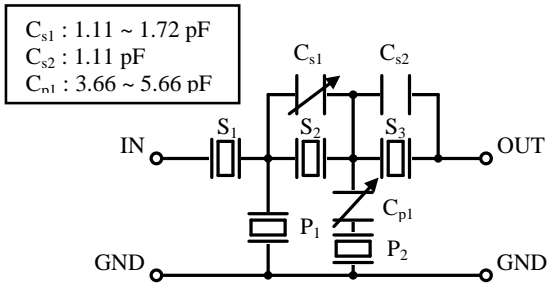
C_{s1} : 1.11 ~ 1.72 pF
C_{s2} : 1.11 pF
C_{n1} : 3.66 ~ 5.66 pF

Figure 1. Circuit diagram of a tunable SAW filter

Upper line

Upper line

Bottom line

Bottom line

Bottom line

Pull-down electrode

(a)

(b)
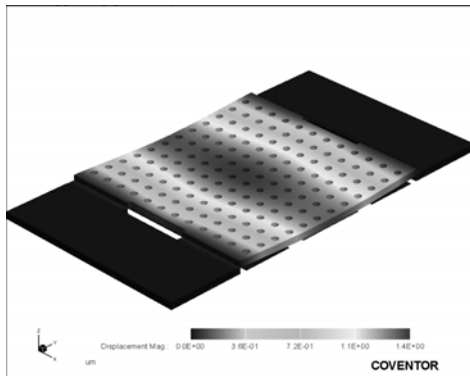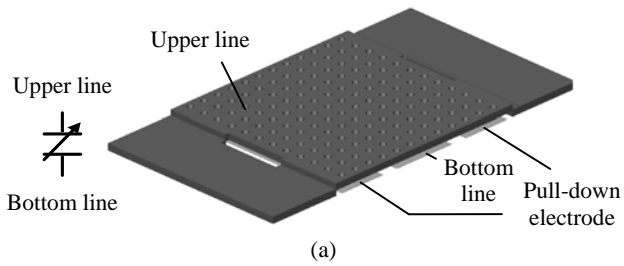
Figure 2. Schematic structure of electrostatically-actuated MEMS variable capacitor (a), and result of FEM simulation (b)

1. Lift off
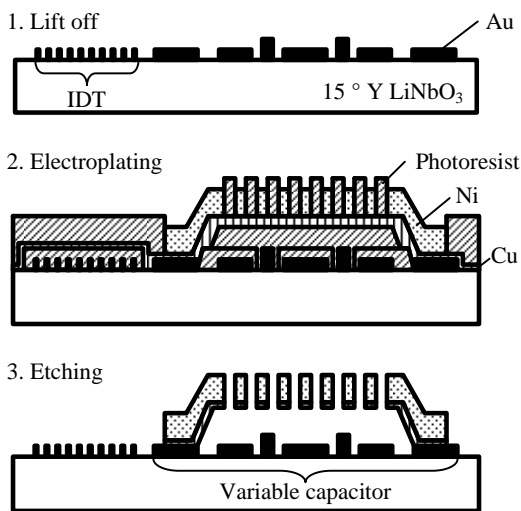
IDT

Au

15 ° Y LiNbO₃

2. Electroplating

Photoresist

Ni

Cu

3. Etching

Variable capacitor

Figure 3. Fabrication process of the tunable Love wave filter on a 15 ° Y LiNbO₃ wafer
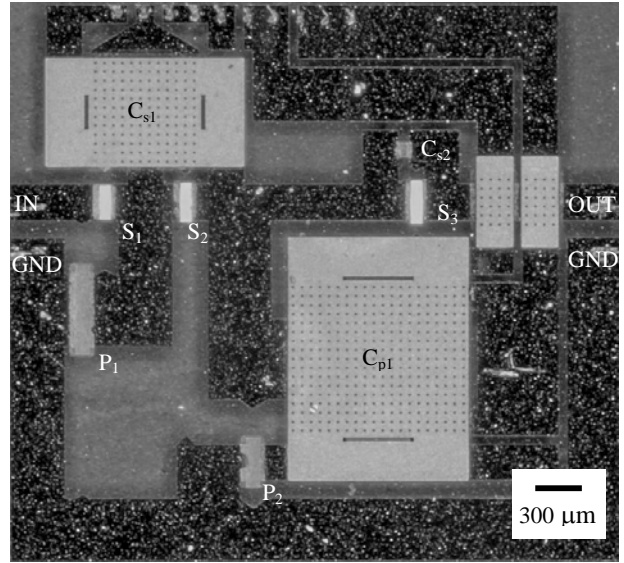
Figure 4. Optical micrograph of the completed tunable filter
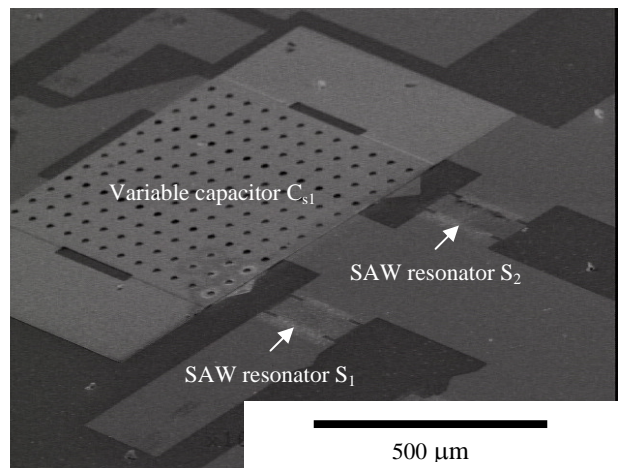
Figure 5. SEM image of the variable capacitor and the SAW resonator
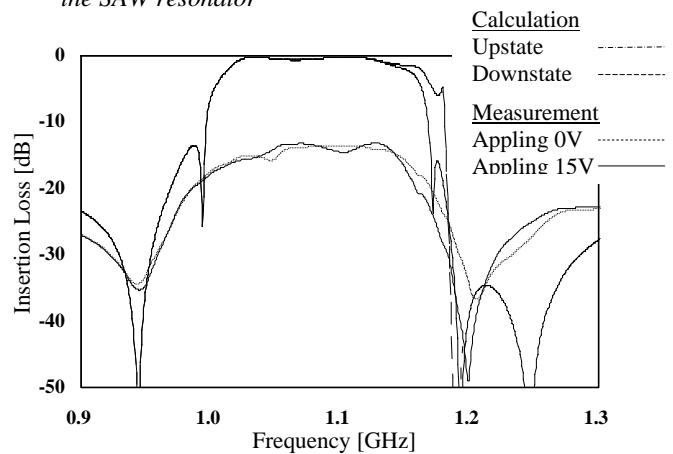
Figure 6. Bandpass characteristic of the tunable filter

WAFER-TO-WAFER TRANSFER PROCESS OF BARIUM STRONTIUM TITANATE METAL-INSULATOR-METAL STRUCTURES BY LASER PRE-IRRADIATION AND GOLD-GOLD BONDING FOR FREQUENCY TUNING APPLICATIONS

Tetsuo Samoto[1], Hideki Hirano[1], Toshihiro Somekawa[2], Kousuke Hikichi[1], Masayuki Fujita[2], Masayoshi Esashi[1] and Shuji Tanaka[1]
[1]Tohoku University, [2]Institute for Laser Technology

This is the first report on successful direct transfer of barium strontium titanate (BST) on a sapphire substrate to a target substrate. Pt/BST/Au metal-insulator-metal (MIM) structures were made on a sapphire substrate, on which (111)-oriented BST was deposited at high temperature (~600°C). The key point of the transfer process is the pre-irradiation of YAG third harmonic laser from the backside of the substrate, which weakens Pt/sapphire adhesion. After the laser pre-irradiation, the BST MIM structures were bonded with Au pads on the target substrate (lithium niobate, LN) at low temperature. Due to thermal expansion mismatch between the substrates, the bonded substrates separated automatically at Pt/sapphire interface during cooling down, and the BST MIM structures were transferred to the target substrate. BST, which has excellent voltage tunability of dielectric constant, is useful for frequency tuning applications in combination with SAW devices and RF MEMS.

A variable capacitor is a key component for frequency tuning applications. BST has excellent voltage tunability of dielectric constant (several hundred % or higher) and low dielectric loss (tan δ) even in GHz range. However, good BST is deposited on R-cut sapphire at temperature as high as 600 °C, and thus basically difficult to use on temperature-sensitive substrates. This is also the case for many functional films, and a laser transfer process was applied to PZT films[1, 2] and AlGaN films[3], but Ref.[1] reported that it did not work for BST due to its high thermal stability. Our Egg-of-Columbus idea is to delaminate Pt, which is used for the seed layer of BST, from sapphire with an assist of laser irradiation. Figure 1 illustrates the process. First, a BST MIM structure is fabricated on a sapphire substrate. The top electrode is Ti/Au, which is used for the following Au-Au bonding. YAG third harmonic laser (λ=355nm, 20ns, 50kHz) is introduced to the BST MIM structures from the backside of the substrate to weaken Pt/sapphire adhesion. Au-Au bonding is performed at 140 °C between the BST MIM structures and Au pads on a target wafer after Ar plasma activation. During cooling down, the bonded substrates automatically separate at Pt/sapphire interface due to thermal mismatch between the substrates. As a result, the BST MIM structures are transferred to the target structure.

For finding a process condition, the dependency of Pt/sapphire adhesion on laser power was investigated by adhesion tape test based on ISO2409. The method and result are shown in Fig. 2, where a threshold laser power around 0.7~0.8W is confirmed. Next, the process illustrated in Fig. 1 was performed with different laser powers. As shown in Fig. 3, the transfer was possible at laser powers higher than 0.8W. The stability and repeatability of the transfer is still low, because the Au-Au bonding was unstable mainly due to particle contamination. In this study, the target substrate was diced LN, which suffers from considerable chipping at the diced edges. Figure 4 shows the transferred BST MIM structure on the LN substrate. No visual damage was observed in the BST MIM structure. Figure 5 shows the Pt surface delaminated from sapphire, where small waviness caused by laser pre-irradiation is found. The mechanism of delamination is not clear, but this waviness might decrease real contact areas between Pt and sapphire.

Figure 6 shows our tunable SAW device on a LN substrate with a transferred BST variable capacitor[4]. This device was fabricated by Si lost wafer process, which can be replaced by the laser-assisted BST transfer process developed in this study. In addition, a similar process may work for other functional films, which are difficult to deposit directly on a device substrate.

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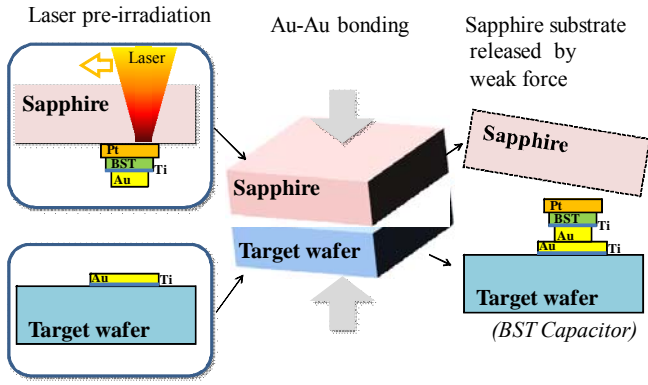[4] H. Hirano *et al.*, IEEE Intl. Ultrason. Symp., pp. 1960−1963 (2011)

Figure 1: Direct BST transfer process with laser-preirradiation. BST MIM structures prepared on sapphire at high temperature are transferred to a target wafer with an assist of backside laser irradiation.
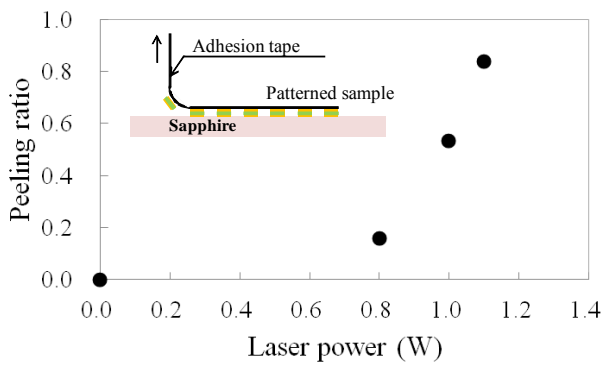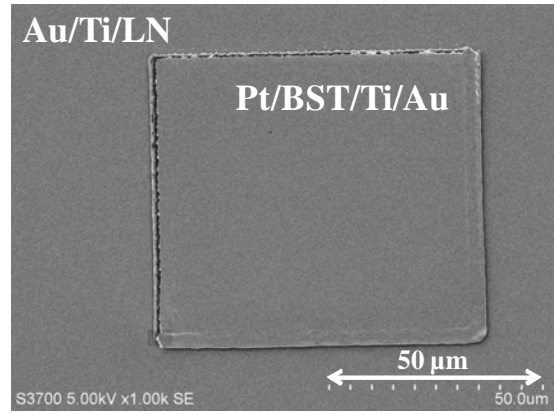

Figure 4: Transferred Pt/BST/Ti/Au MIM structure. The thickness of BST is 200 nm. No visual damage was observed in the BST MIM structure.
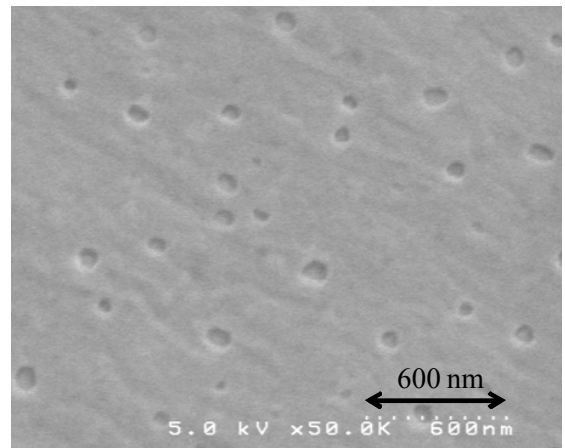

Figure 2: Dependency of Pt/sapphire adhesion on laser power investigated by adhesion tape test (see inset). The sample was the BST MIM structure shown in Fig. 1.

Figure 5: Pt surface delaminated from sapphire, where small waviness caused by laser pre-irradiation is found. Tiny dips were printed from the surface morphology of sapphire.

Figure 3: Dependency of transfer yield on laser power. The transfer was possible at laser powers higher than 0.8W. Unstable transfer was mainly due to particle contamination.
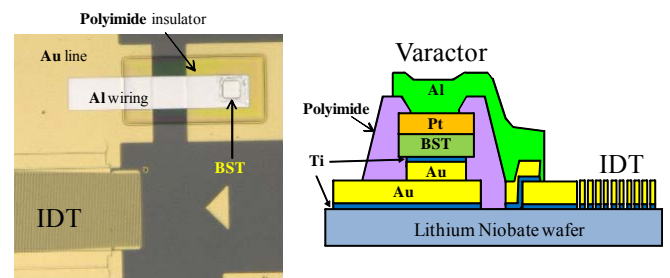

Figure 6: Tunable SAW device with a transferred BST variable capacitor on LN. The BST capacitor was transferred from a Si wafer by lost wafer process, which can be replaced by the laser-assisted transfer process.

WAFER-TO-WAFER SELECTIVE FLIP-CHIP TRANSFER BY STICKY SILICONE BONDING AND LASER DEBONDING FOR RAPID AND EASY INTEGRATION TEST

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Wafer-bonding-type integration can be rapidly and easily tested between different types of devices by our new technology presented here (Fig. 1). Devices to be tested (e.g. MEMS) on a support wafer are bonded and electrically connected with a target wafer (e.g. LSI) using sticky silicone bumps (Fig. 2), and then any of the devices are selectively debonded from the support wafer by backside laser irradiation and transferred to the target wafer (Figs. 3 and 5). A LiNbO$_3$-based SAW device was successfully integrated (Fig. 7) and temporarily sealed with a LSI (Fig. 6), although they have different coefficients of thermal expansion (CTE).

Wafer-bonding-type integration is widely used for inertia sensors etc., because a MEMS and a read-out LSI can be separately fabricated by the best suitable process for each, and also the wafer-level packaging is simultaneously finished. However, actual integration is not easy, partly because the integration process is often complicated, and partly because a wafer-shuttle-based LSI (a few chips of ours on a wafer) must be used in most of early development stages. Therefore, a rapid, easy and chip-selectable integration method is strongly required for device test.

From the above motivation, we have developed wafer-to-wafer flip-chip transfer process using sticky silicone bonding and selective laser debonding, shown in Fig. 1. Partly-similar PDMS bonding[1][2] and laser debonding[3][4] were separately reported, but our study is the first combination of them and the first application to wafer-bonding-based integration and sealing. The devices to be integrated are supported with a glass wafer via a bonding layer of UV resin and a laser-absorbing layer of black resist. On the target wafer (typically LSI), sticky bumps and sealing rings are made using photosensitive silicone, as shown in Fig. 2. For electrical connection, Au/Cr thin film electrodes are made on the silicone bumps. These two wafers are aligned and touched, and the silicone sealing rings immediately bond to the target wafer due to its sticky characteristic. From the backside of the support wafer, YAG third harmonic layer (λ=355nm) is introduced to selectively debond the devices. After separating the support wafer, only the selected devices are left on the target wafer, and the other devices on the support wafer are reusable, because silicone bonding/debonding is reversible.

Figure 3 shows LiNbO$_3$ chips transferred to a Si target wafer, where the silicone sealing rings of different widths (20−350μm) were prepared. The device transfer was possible with the silicone sealing rings wider than 50μm. It should be noted that integration between different materials of substrate is possible, because CTE mismatch problem is relaxed by room temperature process and the elasticity of silicone. Figure 4 shows shear force to separate the transferred device off as a function of the seal ring width. The shear strength is higher than 2MPa, which is enough for device test. The contact resistance at the bumps was measured by four terminal method (Fig. 2), and a mean contact resistance less than 1mΩ was confirmed.

Figure 5 shows the sample where each line was debonded by a predetermined laser power. Only the chips irradiated at a laser power of 0.4W were transferred to the target wafer. If necessary, the transferred chips can be tightly fixed using under-fill polymer, as shown in Fig. 6. After that, standard dicing was possible, and no water intrusion was observed across the sealing ring. For the demonstration of more practical integration, 400MHz SAW resonators on LiNbO$_3$ were transferred to a LSI wafer with CMOS sustaining amplifiers, as shown in Fig. 7. The integrated SAW oscillator successfully worked, showing a very low phase noise of −130dBc/Hz at 10kHz offset and −167dBc/Hz at 1MHz offset.

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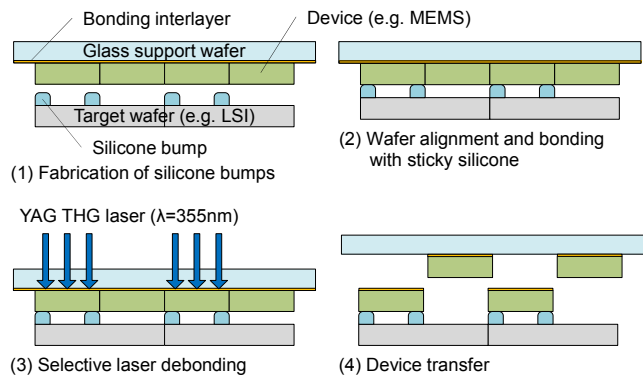[4] Farizah Saharil *et al.*, IEEE MEMS 2010, pp. 47−50

Fig. 1: Wafer-to-wafer selective flip-chip transfer by sticky silicone bonding and laser debonding.
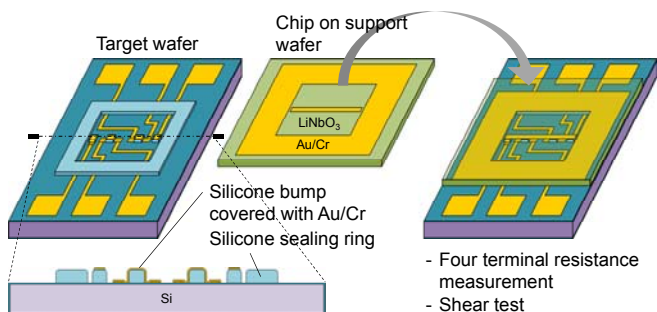

Fig. 2: Structure of samples: target wafer with silicone bumps and sealing ring, and $LiNbO_3$ chip supported on a glass wafer. The integrated sample is subjected to four terminal resistance measurement and shear test (Fig. 4).
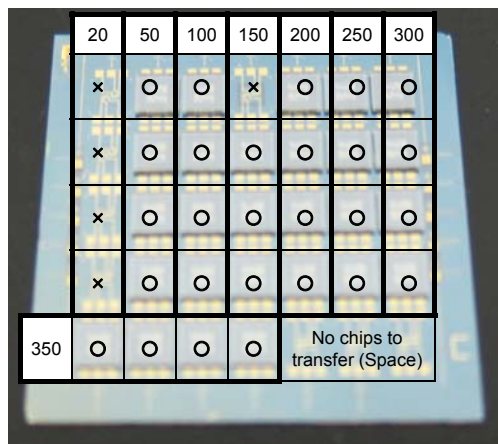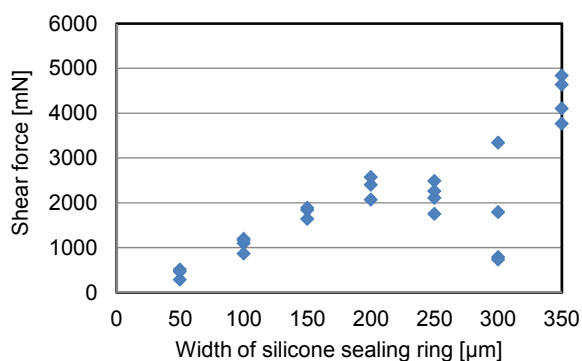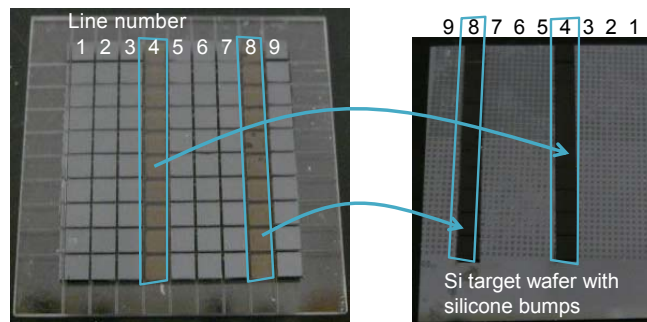

Fig.3: $LiNbO_3$ chips transferred to the target wafer using silicone sealing ring of different widths ($20-350\mu m$). The device transfer was possible with the silicone sealing rings wider than $50\mu m$.

Fig. 4: Relationship between shear force required for chip separation and the width of silicone sealing ring.

#1, 5, 6: No laser irradiation (0W)
#2, 6: 0.3W
#3, 7: 0.35W $\rbrace$ 10mm/s scan at 50µm pitch
#4, 8: 0.4W

Fig. 5: Result of laser debonding at different laser powers (0W, 0.3W, 0.35W and 0.4W for different lines). Only the chips irradiated at a laser power of 0.4W were transferred to the target wafer.
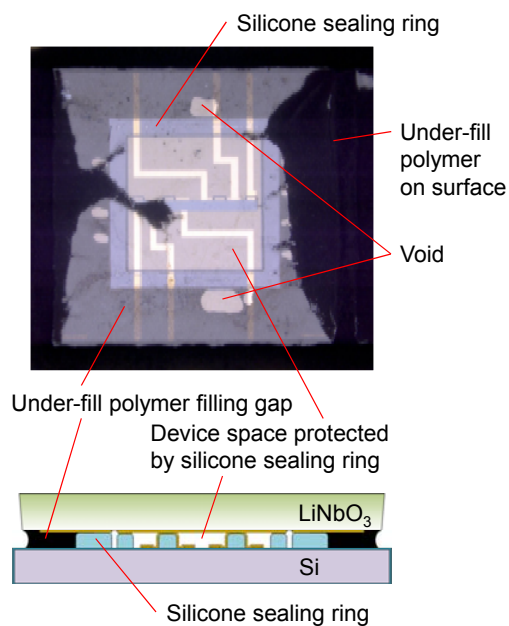

Fig. 6: $LiNbO_3$/Si sample reinforced by under-fill polymer. Standard dicing was possible without damage or contamination inside the silicone sealing ring.
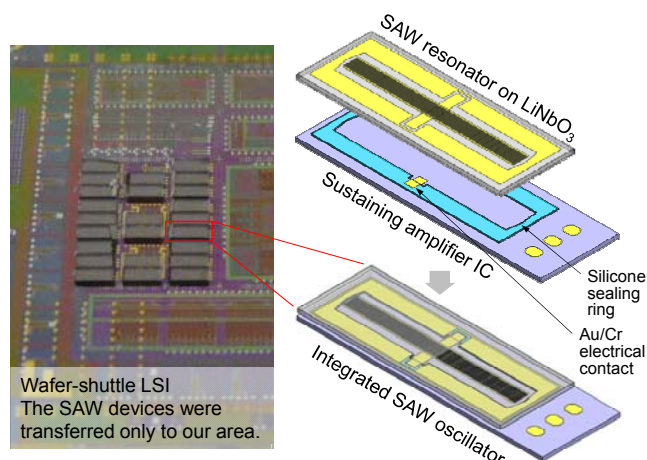

Fig. 7: Integrated SAW oscillator. The $LiNbO_3$ SAW resonators were transferred using silicone bumps and sealing rings. A low phase noise of $-130dBc/Hz$ at 10kHz offset and $-167dBc/Hz$ at 1MHz offset was confirmed at 400MHz oscillation.

WAFER-LEVEL HERMETIC PACKAGING TECHNOLOGY FOR MEMS USING ANODICALLY-BONDABLE LTCC WAFER

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An anodically-bondable LTCC (low temperature cofired ceramic) wafer newly developed by us (Fig. 1) offers a versatile and reliable wafer-level hermetic package with electrical feedthroughs and buried passive components (L, C and R). We confirmed long-term hermeticity of vacuum-sealed cavities by diaphragm method (Fig. 3) even after heat cycle tests (Fig. 4). The width of seal rings necessary for hermetic sealing of saw-diced chips is 0.1 mm or less, which can save chip size (Table 1). Electrical connection between MEMS on a Si wafer and metal vias in the LTCC wafer can be established using Sn-containing metal multilayers simultaneously with anodic bonding (Fig. 5). This electrical connection stands up to a temperature (415 °C) much higher than a melting point of Sn (232 °C), because intermetallic compounds are formed uniformly (Fig. 6). Our anodically-bondable LTCC technology is now ready for commercialization.

Wafer-level vacuum packaging with electrical feedthroughs is one of key common technologies for MEMS. Among many methods which have been developed to date [1], a borosilicate glass wafer with electrical feedthroughs, i.e. metal-plugged via-holes, offers the opportunity of reliable MEMS vacuum packaging by anodic bonding [2]. However, its fabrication has the following difficulties. First, there is no good way to fabricate high-quality via-holes in a sufficiently-thick borosilicate glass wafer at high yield. For example, sandblast is a cost-effective method to fabricate via-holes, but microcracks and tipping deteriorate the quality of via-holes and eventually the reliability of packaging. Second, via-filling with metal is not easy. For example, electroplating is considerably time-consuming.

To solve the above problems, we have developed the novel LTCC wafer anodically bondable with Si (Fig. 1). This LTCC is well matched with Si in CTE, as shown in Fig. 2, and contains sodium ions movable at elevated temperature. Figure 1 shows the cross section of the LTCC wafer. It is made of a stack of punched green sheets, and paste-based metal lines are formed between and through the stacked layers. Thus, not only electrical feedthroughs but also passive components can be embedded in the LTCC wafer.

Anodic bonding between the LTCC and Si is possible with bonding strength equivalent to or higher than that for borosilicate glass on conditions like ≥500 V at 400 °C and 600 V at ≥250 °C. The width of seal rings necessary for hermetic sealing of saw-diced chips was investigated and found to be 0.1 mm or less, as shown in Table 1. We confirmed the reliability of vacuum packaging using a Si diaphragm structure (Fig. 3), and no vacuum level change was observed even after heat cycle tests (−40/+150 °C, 30 min/30 min) at least up to 3000 times, as shown in Fig. 4.

We also developed the anodic bonding method which simultaneously establishes electrical connections between the LTCC wafer and a Si wafer. As shown in Fig. 5, a low-melting-point metal is patterned with other metals on Au vias in the LTCC wafer as it sufficiently reaches the counter metal pads. The recommended protrusion height is 0.5 μm to 1 μm. After aligning both wafers, the wafer set is heated up to bonding temperature in a short time (e.g. 1~10 min), and high voltage is applied. The low-melting-point metal once melts and forms intermetallic compounds with other pad metals [3]. We demonstrated this technology using Sn/Cu/Cr + Cr/Ti system. Figure 6 shows the cross section and composition of the connected metal pads. Judging from the composition (Sn : Cu ~ 1 : 1), this metal connection has a remelting point of 415 °C, which is sufficiently higher than reflow temperature for device mounting on a printed circuit board.

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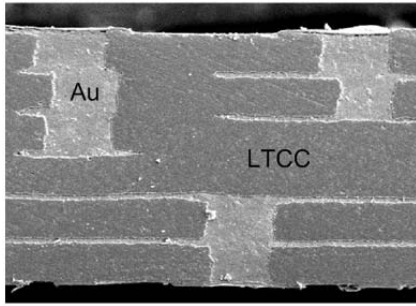
Fig. 1 Cross section of anodically-bondable LTCC wafer with 7 layers
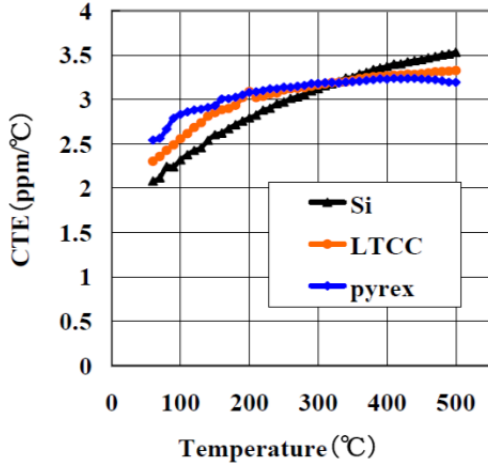

Fig. 2 Comparison of the coefficient of thermal expansion (CTE) of Si, LTCC and Pyrex glass
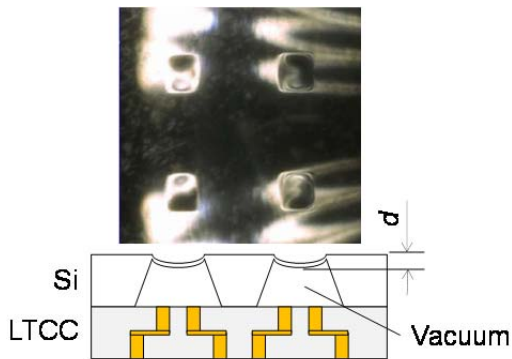

Fig. 3 Diaphragm method to evaluate long-term leak rate; The diaphragm is made of p++ Si.
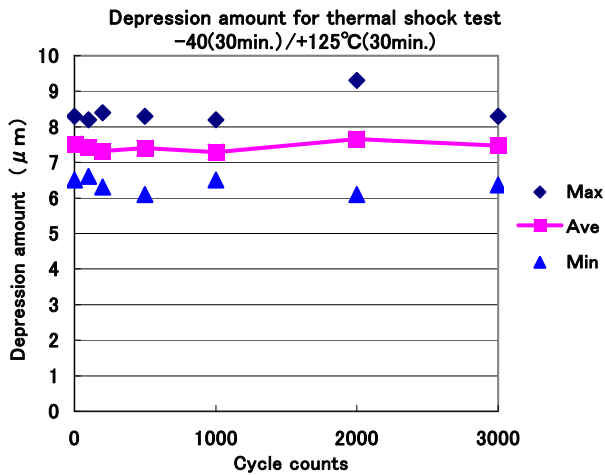

Fig. 4 Diaphragm deformation during heat cycle test (−40 °C/+125 °C, 30 min/30 min); No obvious change of the diaphragm deformation was found at least up to 3000 cycles.
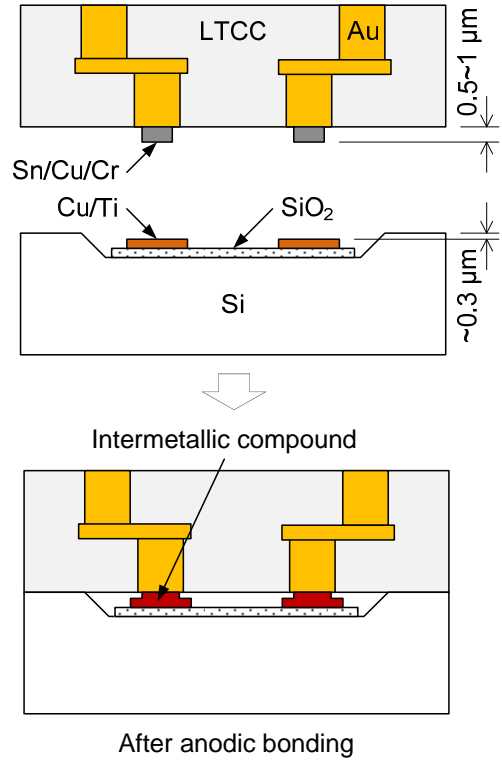

Fig. 5 Electrical connection between MEMS on Si and vias in LTCC using Sn/Cu/Cr + Cu/Ti system; The electrical connection is established in parallel with anodic bonding.
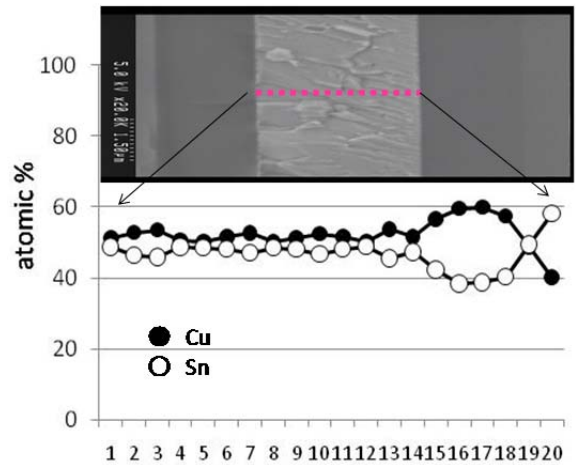

Fig. 6 Cross section and composition of the electrical connection; The structure and composition are almost uniform along the thickness direction. The remelting temperature of the electrical connection is 415 °C judging from the composition.

Table 1 Dependency of leak rate on the width of seal ring of saw-diced chip; Both LTCC-capped and glass-capped chips achieved sufficiently small leak rate.

Width of seal ring (mm)	Leak rate for LTCC (Pa m^3/s)	Leak rate for birosilicate glass (Pa m^3/s)
0.1	$\leq 2.2 \times 10^{-12}$	$\leq 1.1 \times 10^{-12}$
0.2	$\leq 1.8 \times 10^{-13}$	$\leq 1.8 \times 10^{-13}$
0.3	$\leq 3.3 \times 10^{-12}$	$\leq 2.2 \times 10^{-12}$
0.4	$\leq 2.4 \times 10^{-12}$	$\leq 8.8 \times 10^{-13}$
0.5	$\leq 7.0 \times 10^{-13}$	$\leq 1.7 \times 10^{-12}$
0.5	$\leq 3.5 \times 10^{-13}$	$\leq 1.0 \times 10^{-12}$

STOCHASTIC GRAVITY SENSOR WITH ROBUST OUTPUT USING WHITE-NOISE-APPLIED BI-STABLE STATE FOR LOW S/N ENVIRONMENTS

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We demonstrated a stochastic gravity sensor **(Fig. 2 (a), (b))**, which just counts the number, m, of pull-in to either of counter electrodes in n-times trials to know pull-in probability, m/n, under white-noise-applied bi-stable state **(Fig. 1)**. This new sensing principle is robust against noise and parasitics, which severely limit sensor performance in such a low S/N situation that the sensor in a harsh environment is connected with a read-out circuit using a long wire. Pull-in to the counter electrode resulted in large capacitance change, and clear sensing signal **(Fig. 4)** was observed at *Ch*.1 **(Fig. 2 (a))** even under low S/N condition. We confirmed the sensing principle by both simulation and experiment. The sensing range can be tuned by bias voltage applied to the counter electrodes (V_{bias}) **(Fig. 5 (a))**, and even small gravity can be measured by the probability of pull-in **(Fig. 5 (b))**. For example, a sensing error of 10^{-3}G at $\pm 3\sigma$ accuracy is obtained by 2290-times trials. Higher accuracy is easily obtained just by increasing trials.

Sensing gravity to know direction and inclination is important for geothermal well drilling [1]. However, to use MEMS sensors in such a harsh environment is difficult, because a typical silicon read-out circuit cannot be used above 150 °C. Thus, the read-out circuit must be in a low-temperature environment and connected to the MEMS sensor using a long wire. However, this is also a problem especially for capacitive sensors due to large parasitics (*C, L* and *R*). As one of promising solutions of this problem, we demonstrated the new sensing principle that the probability to fall into either of bi-stable position depends on the gravity force applied to the sensor under white-noise-induced vibration (Fig. 1). Figure 2 shows the schematic structure. The mass supported by springs is randomly oscillated by white noise, and a pulse voltage (V_p) applied to the mass changes the mono-stable state (random vibration) to the bi-stable state. A similar sensing principle was demonstrated just using silicon transistors [3], but clearly this does not work at high temperature (> 150 °C).

The sensing principle was first confirmed by simulation based on a physical model, and then the sensor was prototyped on a glass substrate using an anodically-bonded thin Si layer (Fig. 2 (b)). Figure 3 shows the fabricated sensor. For reliable pull-in and release action, a non-linear spring structure (Fig. 3 (b)) was made to produce restoring force sufficiently larger than electrostatic force caused by the bias voltage and white noise. For detecting pull-in, a sinusoidal signal was applied to the mass, and this signal was detected at one of the counter electrode (*Ch*. 1 (Fig. 2)). Figure 4 shows an example of the burst pulse wave (V_p) detected at *Ref*. (Fig. 2) and the amplitude of the sinusoidal signal detected at *Ch*. 1. At *Ch*. 1, pulses (red) appeared stochastically, synchronizing burst pulse wave at *Ref*. (V_p, blue). Each red pulse corresponds to pull-in to the upper electrode.

Figure 5 shows an example result of gravity measurement using the fabricated sensor. The sensing range can be tuned by the bias voltage applied to the counter electrode ($V_{bias-upper}$) (Fig. 5 (a), Rough sensing mode), and the probability of pull-in to the upper electrode depended on applied gravity (Fig. 5 (b), Accurate sensing mode). At $V_{bias-upper} = -1.02$ V and $V_{noise} = 10$ V$_{p-p}$, for example, a sensing range is ± 0.08G and a sensing accuracy of 10^{-3}G at $\pm 3\sigma$ accuracy is obtained by 2290-times trials. Higher accuracy is easily obtained just by increasing trials.

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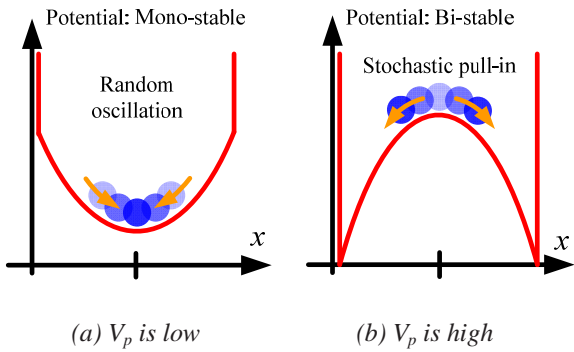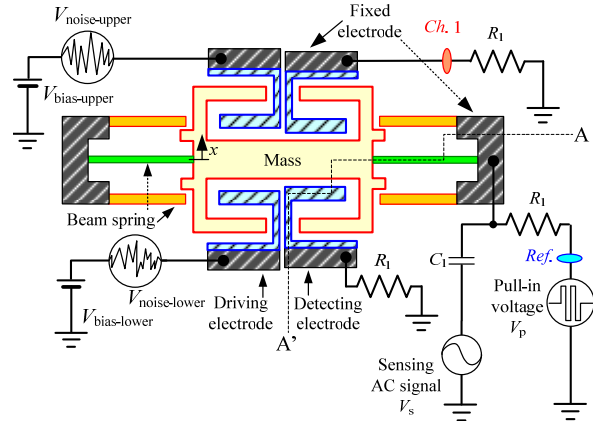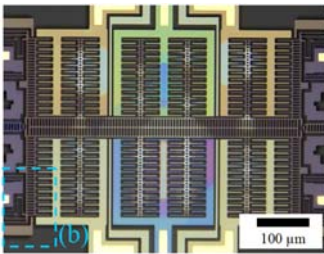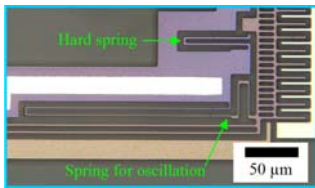
(a) V_p is low   (b) V_p is high

Figure 1: Two kinds of mass potential state dependent on pulse voltage (V_p) applied to the mass

(a) Overall view

(b) Magnified view of the spring part
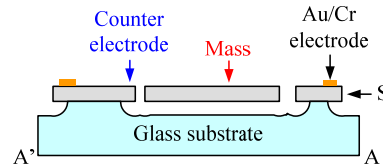
Figure 3: Micrographs of the stochastic gravity sensor fabricated using a thin silicon layer anodically-bonded on a glass substrate

(a) Rough sensing mode   (b) accurate sensing mode

Figure 5: Measurement result of stochastic gravity sensor
(a) Relationship between the sensing range of gravity and upper bias voltage
(b) Relationship between the probability of pull-in and gravity under $V_{bias-upper}$ fixed

(a) Configuration of the stochastic gravity sensor

(b) Cross-sectional structure of the stochastic gravity sensor

Figure 2: Configuration and cross-sectional structure of the stochastic gravity sensor
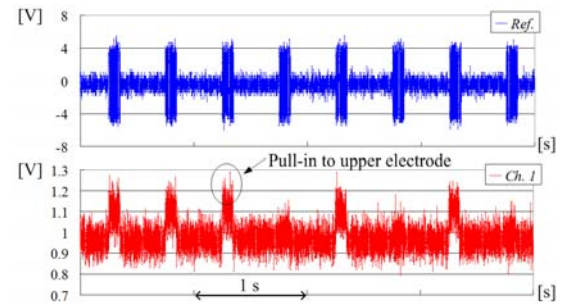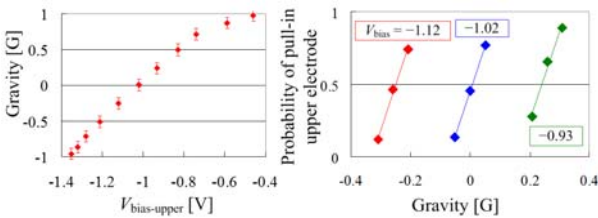

Figure 4: Stochastic pull-in to the upper counter electrode
<Upper chart> Burst pulse signals applied to the mass (detected at Ref. in Fig. 1) for pull-in
<Lower chart> The amplitude of sinusoidal signal detected at the counter electrode (Ch. 1 in Fig. 1)